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DESIGN OF A CHARGE PUMP-BASED BODY BIAS GENERATOR FOR FDSOI CIRCUITS

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Advisor: Francesc de Borja Moll Echeto

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Title of the thesis: DESIGN OF A CHARGE PUMP-BASED BODY BIAS GENERATOR FOR FDSOI CIRCUITS

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Abstract

Electronics circuits powered at near-threshold voltages (ultra-low voltage designs) are desirable for their low power consumption. However, the performance at such voltage supply is degraded. The application of forward body bias to the circuit can counteract the performance loss. FDSOI is a suitable technology to these techniques, due to its high range of body bias voltages. To generate that body bias voltages, positive and negative, charge pumps circuits are designed to be integrated on the chip. This thesis studies the main challenges on the design of such circuits operating at 300 mV to reach voltages of ± 1 V with power consumption lower than 1 μW and how to model it for layout process. In addition, a control circuit is also designed to provide different intermediate body bias voltage.

To my family, without them anything of this cannot be possible. To my parents, for their unconditional believe in me all these years. To my brothers, despite the distance between us, we always stay together.

To Ana for her support all these years and for doing each day better than last one.

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1

INTRODUCTION AND OUTLINE

1.1. Introduction

In today's society, portable devices are more and more present in all fields of usual life, for example, on communications, biomedical, sports and automatic process. One of the reasons being for the increase of portable electronics is the shrink of components, explained in Moore's Law [1], allowing to make smaller devices with the same functions.

Another reason for the growing number of hand-held devices, is the development of telecommunications that provides newer and powerful ways of communication between devices and Internet. One of the most important increase on the number of portable electronics, in the last and next years, is due to Internet of Things. In Figure 1 is shows the statistics of the last years and forecast for the upcoming years [2].

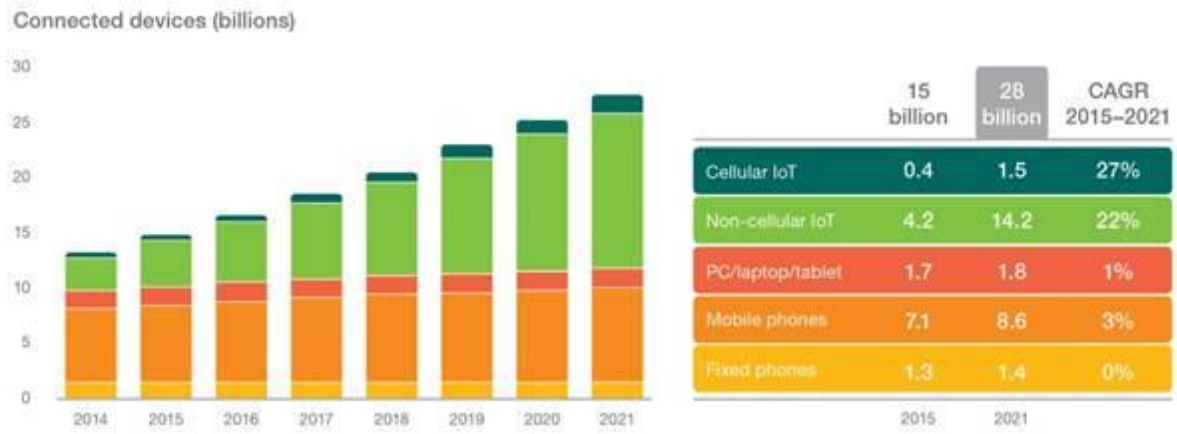

Figure 1. Trend of IoT devices [2]

In the development of new and power portable systems, however, a main limitation appears, the energy and power consumption. With the evolution of hand-held devices, electronic and software applications increase their performance, therefore the power consumption increases, but batteries do not grow up proportionally due to physical limitations. This reduces batteries' lifetime.

As new technologies are developed for power supply portable devices, a new trend of design electronics devices is used, the low-power techniques. One of the low-power supply is based in the reduction of supply voltage of the circuits, coming down to values near-threshold voltage of transistors. Low-power design is complementary to others techniques to increase battery's lifetime of portable devices.

As other solutions, low-power design has advantages and drawbacks. Minimizing the voltage of power supply, until near-threshold voltages, has the advantage of a drastic reduction in energy and power consumption [3]. The new level of consumption enables the use of new sources of energy, like harvesting, to power supply the new electronic devices.

On the other hand, the drawback of working in near-threshold voltage is the exponential increase in the gate delay, degrading performance of electronics devices, limiting the functions applicable to such components.

To counteract the loss of performance when low voltages are applied, the use of forward body bias is one technique applied to reduce the threshold voltage, effectively increasing overdrive voltages which are nominally near- or even sub-threshold [4].

To achieve better control of the mechanism for the forward body bias (FBB), for this project, FDSOI technology with Ultra-Thin Body and Buried oxide (UTBB) is used. This FDSOI technology allows a large range of body bias voltages, up to 2V [5].

In this document it is proposed the electrical design of a body bias generator (BBG) with the FDSOI UTBB technology. This master's thesis is a continuation of a research project started in the third semester of the Master in Electronics Engineering, within the subject of Introduction to Research. This research was presented in XXXII Conferences on Design of Circuits and Integrated Systems, DCIS, in November 2017 [6].

This voltage generator is going to be based into a charge pump structure and some of the requirements are:

- The voltage of the power supply shall be 300 mV, to be in the near-threshold voltage of the technology;
- The voltage generated by the design shall be at least ±1 V, to be used as forward body bias for other circuits and feedback itself;
- The body bias generator shall be regulated, to be capable of turn on and turn off the generator or to create a range of voltages to be used in different states and situations;
- The power consumption of the body bias generator shall be lower than 1 µW, when ±1 V is generated;
- It should be desired to test physical capacitors in the electrical design of the body bias generator.

Once the BBG's design is simulated, it is proposed the design of a circuit of control. This electrical circuit shall manage the voltage generated by the BBG, at least to control the generation of 1 V. It should be desirable that the control circuit could be extended to manage the generation of more values of voltage.

For the design and simulation of the entire electrical design, the software tools of Cadence and the library of the FDSOI UTBB are used.

1.2. Outline of the Thesis

This thesis is organized as follows. The second chapter presents an introduction to the history of low-power voltage design. Third chapter briefly introduces FDSOI UTBB technology of 28 nm, which is the technology used in this thesis for the electrical design of the body bias generator and the control's circuit. Chapter four explains the state of the art of actual charge pumps is explained and how finally it is decided to use it to create the voltage generator of the design.

On fifth chapter, the design of the body bias generator is presented and all blocks of the electrical design are explained as well as their function, how they are made and tested. Once all the BBG is explained, the optimization process is shown with some results.

On chapter six, an approach to the design of the control's circuit is shown, presenting in detail the functional idea, the process of design, how it is created and the results of the simulation of this part of the circuit.

Seventh chapter shows the simulation results of the body bias generator and of the control's circuit in the same circuit.

Chapter eight explains the replacement of the ideal capacitors of the body bias generator for physical capacitors and shows new simulations with these real components.

In chapter nine the financial study of the project is included, analyzing the personal and materials needed to do it. Finally the thesis is concluded in chapter ten.

1.3. Gantt Chart

This section shows the plan of development of the thesis, where all tasks are defined and explained. To build-up the project, software tool Microsoft Project was used.

	Nombre de tarea	Duración	Comienzo	Fin
1	**Design of the Body Bias Generator**	**58 días**	**lun 03/07/17**	**mié 20/09/17**
2	Design of the functional model	23 días	lun 03/07/17	mié 02/08/17
3	Study of the effect of the Forward Body Bias	13 días	jue 03/08/17	lun 21/08/17
4	Optimization of the Body Bias Generator	22 días	mar 22/08/17	mié 20/09/17
5	**Design of the Control Circuit**	**94 días**	**jue 21/09/17**	**mar 30/01/18**
6	Design of the frequencimeter	25 días	jue 21/09/17	mié 25/10/17
7	Study of the control with the different Body Bias	13 días	jue 26/10/17	lun 13/11/17
8	Design of the clocks of the frequencimeter	4 días	mar 14/11/17	vie 17/11/17
9	**Analysis of the complete circuit**	**39 días**	**lun 20/11/17**	**jue 11/01/18**
10	Design of a Body Bias of 1 V	21 días	lun 20/11/17	lun 18/12/17
11	Analysis of results	18 días	mar 19/12/17	jue 11/01/18
12	**Thesis of the Master**	**31 días**	**mar 19/12/17**	**mar 30/01/18**
13	Redaction of the thesis	23 días	mar 19/12/17	jue 18/01/18
14	Presentation of the thesis	8 días	vie 19/01/18	mar 30/01/18

Figure 2. Tasks of the project

During the project build-up, apart from tasks of the thesis, some meetings with Professor Francesc Moll were scheduled every week or every two weeks, excepting vacation periods. These meetings were used to show the project's progress, doubts and problem solving.

Tasks are show in Figure 2 and the distribution in time of each task is shown in Figure 3.

In respect of the initial base line, most of the tasks were completed within deadline, except task 13 and 14 of Figure 2, that had a delay of two weeks.

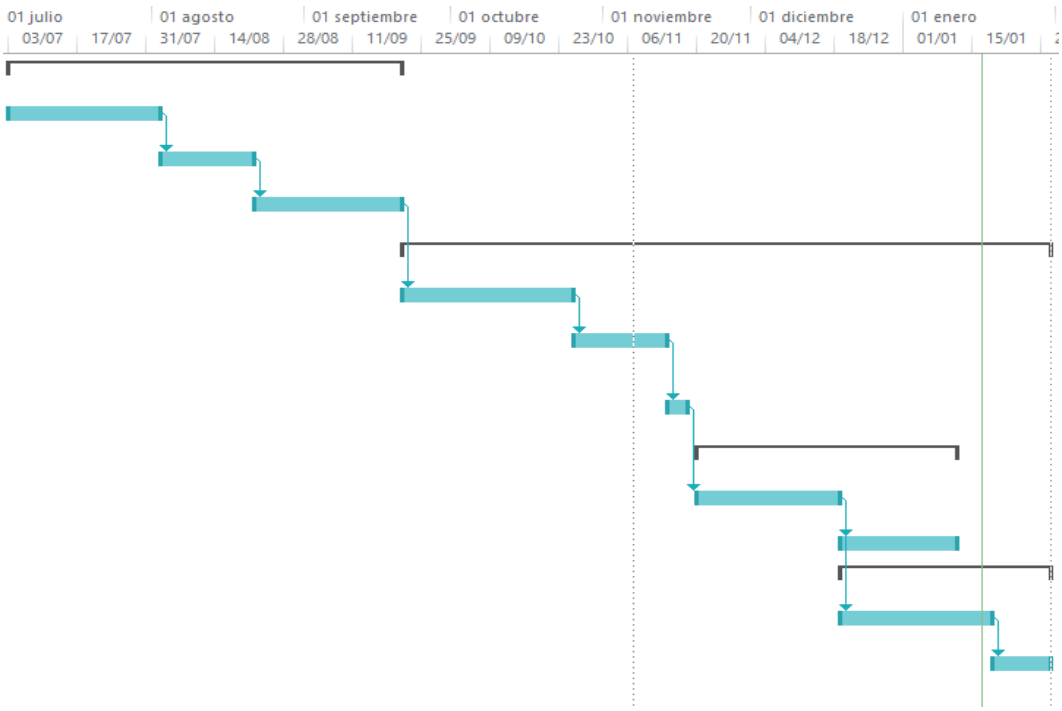

Figure 3. Time's distribution of tasks

2

LOW-POWER VOLTAGE DESIGN

2.1. Introduction

In 1965, Gordon Moore predicted that the transistors inside a chip would double every 18 months, at least for the next years [1]. Moore's law was created and verified with the time. If we observe the evolution of CMOS technology, the scale factor between technology nodes is reduced approximately in a 30%, to pack the double of transistors in the same area of chip [7].

With the first technologies, the use constant voltage to supply the transistors was the preferred technique, thus the newer technology was compatible with last technology. That compatibility allows to reuse and export ancient circuits, accelerating the design's process [8].

But with 0.6 μm technology node, the supply voltage has been scaled down in every technology node. The reason is that with the reduction of technology node, more transistors are in the same area, making that power density increases. Such increment in the power density causes that the integrity of the devices was poor, risking the devices breakdown [8].

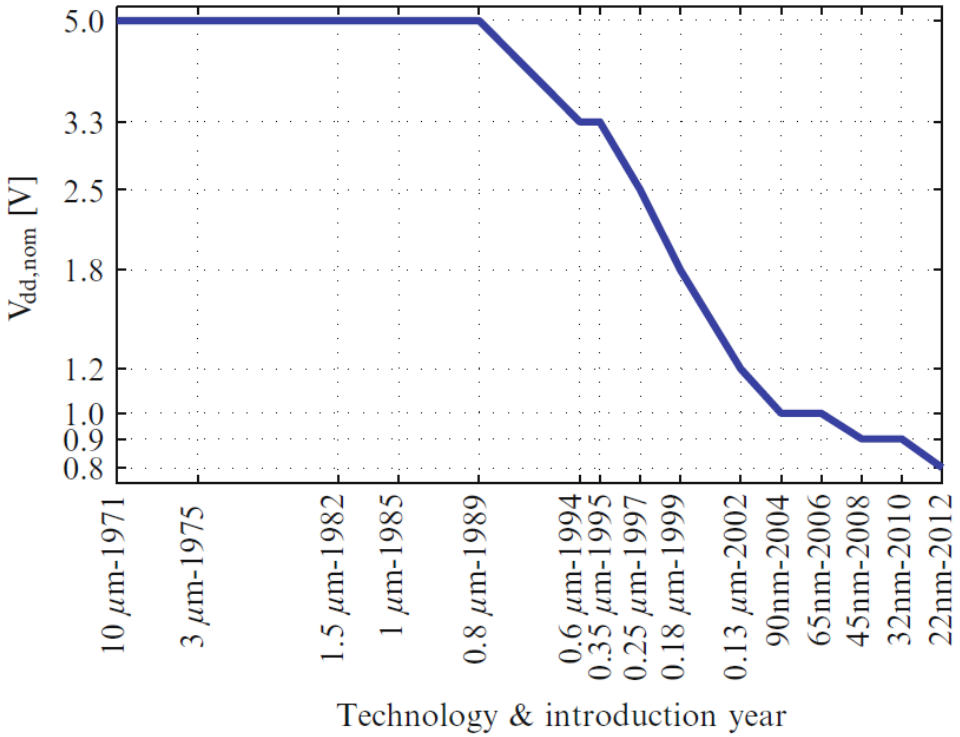

Figure 4. Scaling of supply voltage in relation with CMOS technology nodes [8]

To solve this problem, in 1974, Dennard proposed Constant Electric Field (CEF) scaling [9]. In this theory, voltage and geometry of technology node shrink proportionally to compensate the electric fields and make it constant, thereby the power density is constant, avoiding breakdown risk of devices.

This theory is accomplished, until the 90 nm technology node, when scaling of voltage supply slows down, as shown in Figure 4 [10] [11]. The reason is that for nanometer technologies, the leakage power becomes more important. To accommodate to different functionalities of designs, foundries offer new technology nodes with low-leakage.

2.2. Ultra-Low-Voltage Design

The ideal behavior of transistors is to work as a switch, that could conduct or not depending the voltage applied. The voltage that limits the two ideal position, on and off, is called threshold voltage, V_T. In the theoretical model, when the voltage applied is above V_T, the transistor allows the conduction of current and the value is below, transistor is turned off and blocks the current.

In real model, the transistor doesn't turn off just below of the V_T, it just reduces exponentially the current that passes through the channel in order to the voltage applied. This variation in the behavior in respect to ideal model, allows to work with voltages in range of sub-threshold value [8].

The main advantage to work with that near-threshold voltage is the drastic reduction of power and energy consumption. But that functional region of transistors produces delay in the circuits, due to the current between drain and source of the transistor, called I_{DS}, is lower than in over threshold region. Another drawback is the increase of sensitivity to variations of transistors, making difficult to define exact values of the transistors' properties.

Another fact to take consider when transistors work in near-threshold voltage, is the importance of the leakage current, noted as $I_{leak.}$ It is caused by the reduction of the I_{DS} of transistors when it works in that functional region, making that both values, I_{leak} and I_{DS}, could be comparable.

In the last years, especially in XX century, the research about ultra-low-voltage design achieved more importance due to the growing number of portable devices and the power problems caused by scaling of the CMOS technology. Figure 5 shows the increment of the number of publications in the last years and its rising trend.

In the first steps of research in this field, the main focus was to reduce the power and energy consumption, to extend battery life of the devices. But when the portable applications become more complex, the research also focuses on the increase of performance of the designs, due to delays of the circuits, the achieved working frequencies of devices were too low.

One of the future challenges of the ultra-low-voltage design is to make this field to be widely adopted by industry, because nowadays the applications are more in the academia. To achieve this goal, it is necessary to achieve robustness of transistors, guaranteeing a high

yield through high variation of the system. Another objective is to achieve that the working frequencies of circuits are higher, at least some tens of MHz [8].

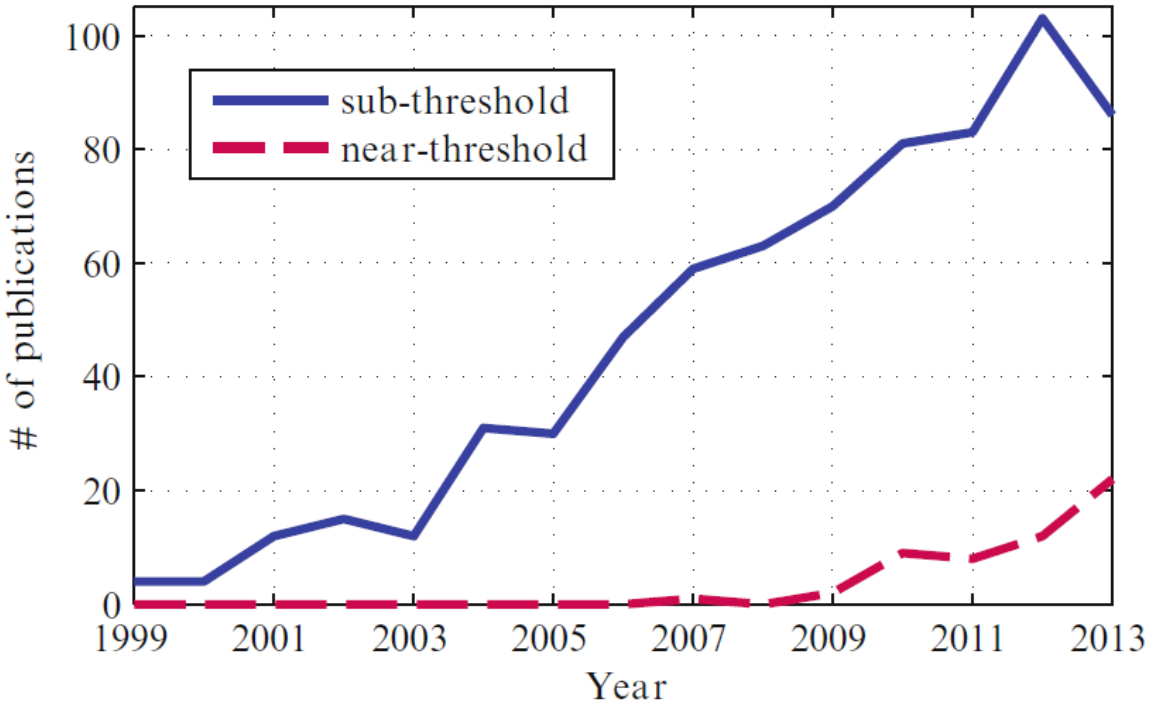

Figure 5. Trend of publications about sub- and near-threshold designs [8]

2.3. Effects of body bias in the threshold voltage

As explained in the Section 2.2, the threshold voltage, V_T, is a characteristic of the transistor, which denotes the transition between conduction, strong inversion region, and not conduction, weak inversion region. The equation to define the threshold voltage is the following:

$$V_T = V_{T0} + \gamma\left(\sqrt{\emptyset_0 - V_{bs}} - \sqrt{\emptyset_0}\right) - \eta \cdot V_{ds} - \Delta V_T \text{ [8]}$$

, where V_{T0} is the threshold voltage for bulk-source voltage V_{sb} equal to 0; the second factor, $\gamma\left(\sqrt{\emptyset_0 - V_{bs}} - \sqrt{\emptyset_0}\right)$, is due to the body effect; the third factor, $\eta \cdot V_{ds}$, is due to Drain-Induced Barrier Lowering, denoted as DIBL; and finally the last factor, ΔV_T, caused by the short channel effect. In this thesis, the focus is the factor of body effect.

If the terms affecting the body effect are studied, all of them are defined by the technology and fabrication of transistors, except the bulk-source voltage, V_{bs}. The voltage V_{bs} is the major influence on V_T.

To explain the effect of V_{bs} on V_T, a NMOS transistor is used as a model. If a negative voltage V_{bs} is applied, the amount of charge required to invert the channel is increased, in consequence the V_T also increases. This is denoted Reverse Body Biasing (RBB). In other case, if a positve voltage V_{bs} is applied, the V_T decreases. This is called Forward Body Biasing (FBB). If the transistor used is a PMOS, the RBB is applied with positive voltage V_{bs} and the FBB is applied with negative voltage V_{bs}.

The manipulation of the threshold voltage by body biasing becomes more useful in newer technologies, as the Fully Depleted Silicon-On-Insulator. The reason is that these new technologies allow a better control of voltage of body biasing [6] [8].

The use of body biasing is a trend to use in ultra-low-voltage-design. By using this technique of manipulation of threshold voltage, circuits increase their performance, higher working frequencies, at the expense of increase the leakage.

2.4. Types of transistors

Around the 120 nm technology node, foundries started to offer different technology options: high-performance and low-leakage. For some technologies, it is possible to use both options in the same wafer [8].

Other CMOS technologies also offer multiple V_T-options and the selection of threshold voltage. The most common technologies offer three types of transistors:

- Low-V_T or LVT transistors. They have the lowest threshold voltage and are used in applications that require highest speed.
- High- V_T or HVT transistors. They have the highest threshold voltage and are used in applications where leakage power is an important factor to reduce.
- Standard-V_T or SVT transistors. They have an intermediate threshold voltage and are used in applications that required medium speed and the problems of power safety are not so important.

3

28 NANOMETER UTBB FDSOI TECHNOLOGY

3.1. Introduction to FDSOI

Increasing demand of portable devices are pushing the foundries to improve new technologies to improve logic performance with low voltage supply. To enlarge the battery lifetime, static and dynamic power have to be reduced. However, the Bulk-Si devices have physical limitation when it is under sub-micrometer region. One of the problems is the increase of gate tunneling current as the gate insulator becomes thinner with smaller technologies. The thinner insulator makes that junction leakage increase at the same time as the technology node shrinks [12]. One of the best alternatives to bulk technology is Fully Depleted Silicon-On-Insulator technology, denoted as FDSOI [13]. Figure 6 shows the structure of MOSFET based in Bulk-Si and FDSOI technology.

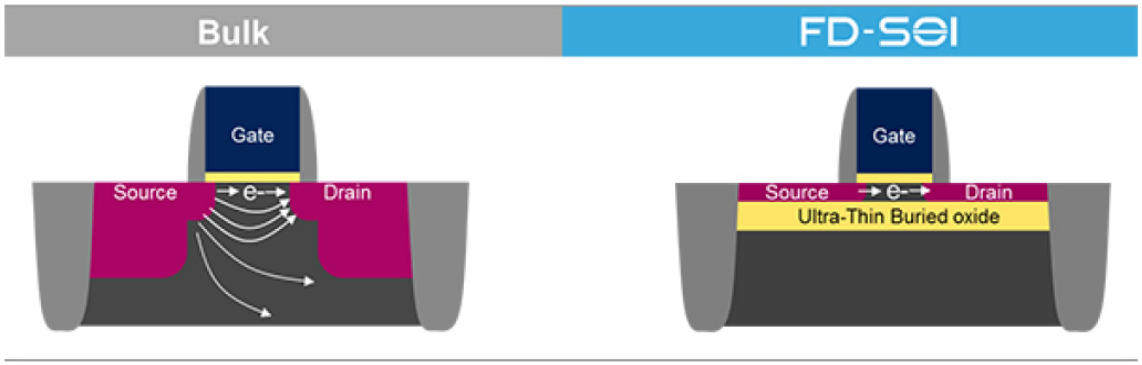

Figure 6. Bulk-Si and FDSOI MOSFET [13]

FDSOI technology is part of ultra-thin film devices. In this case, FDSOI has an ultra-thin layer of silicon over a Buried Oxide, called as BOX. The top silicon layer doesn't have any intrinsic charge carriers and it denoted as a layer fully depleted. One of the variations of FDSOI technology is the Ultra-Thin Body and Box and its main difference in the structure, the thickness of the Box is 25 m or less, instead the 150 nm of thickness of normal FDSOI technology.

3.2. Advantages of UTBB FDSOI

As an alternative to Bulk-Planar technology, some favorable characteristics belongs to UTBB FDSOI. Some of the principal advantages are [14]:

- This technology has better transistors electrostatics, it means, it improves transistor parasitics and the behavior of transistor, especially at low voltage supply; and the variability sources are reduced.
- It provides lower gate leakage current, solving the scaling problem of Bulk-Planar technology. It is possible because it has a thicker gate dielectric and because the leakage current of FDSOI is less sensitive to temperature.
- FDSOI also has lower channel current leakage, due to the carriers are efficiently confined from source to drain.
- The fabrication process is 90% compatible with 28nm Bulk-Planar technology, then it is possible to use the same manufacturing tools. To solve the initial problem of cost, several process steps and masking are removed. Another characteristic of the compatibility in the manufacturing process, is that the design process is also very similar.
- Body bias techniques could be applied to FDSOI, allowing dynamic modulation of threshold voltage. It makes this technology suitable for devices that need high speed of logic and high efficiency.

3.3. Modulation of threshold voltage in UTBB FDSOI

UTBB FDSOI is one of the most suitable technologies to be used in ultra-low voltage design of electronics devices. The reason is the capability of manipulation the threshold voltage of transistors. UTBB FDSOI MOSFET could modulate its own V_T by several ways [14].

The first option to tune the threshold voltage of transistor is the gate oxide. This option varies the thickness of the oxide of the transistor's gate, modifying the characteristics of transistors. It allows to specify the nominal voltage of the devices, where more thickness oxide increases this value.

The next option is the implant of a ground plane, which suppress the depletion depth below the BOX, achieving a better DIBL; it improves the effect of the body bias and produces a variation of 80 mV of threshold voltage of transistors. To adjust the V_T, the implant of ground plane is used at the same time with the flip of the well or not, it depends of the type of transistor used. To improve the results, usually the RVT transistors are used with the standard well and the LVT transistors with the flipped well. The RVT option is used to reduce leakage and the LVT is used to increase the speed. The last fabrication option to tune threshold voltage is the polybiasing, which could be selected in the modelling, but once it is fabricated, it cannot be modified.

Beside the fabrication factors to tune threshold voltage, a dynamic technique can be applied to UTBB FDSOI, the body biasing. The focus of the thesis is to use body bias techniques to modify the V_T. The procedure of this strategy is to apply some voltage just below the BOX of the desired transistor. As it is explained in Section 3, FDSOI technology allows to implement forward body bias and reverse body bias, depending on the focus of the electronic design.

3.4. Selection of Low Threshold Voltage transistors

In this thesis, the transistor selected to make the electrical design of the body bias generator are the LVT transistors with flipped well and ground plane. The structure of this type of transistor is shown in the Figure 7.

The selection of LVT transistor is chosen because it provides a good performance with voltage supplies near-threshold voltage. It is important to achieve the design of powerful and complex designs, achieving working frequencies above 100 MHz for a voltage supply of 300 mV.

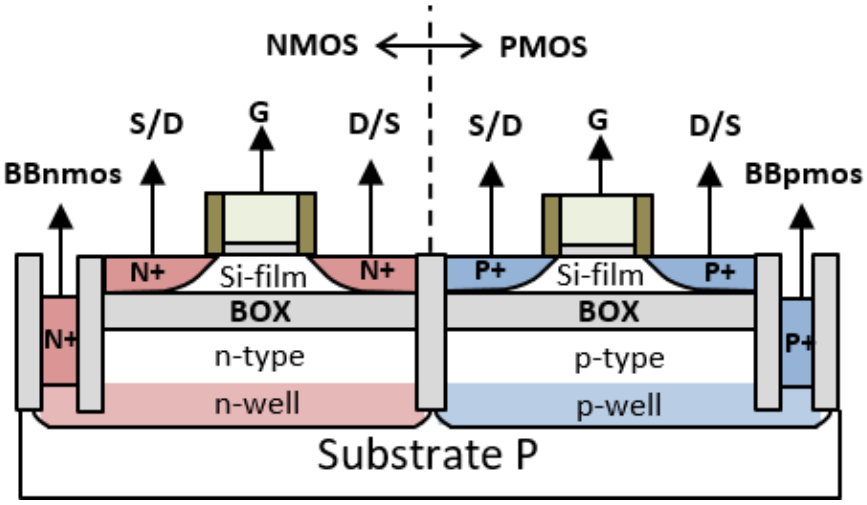

Figure 7. LVT transistor with flipped well and ground plane in UTBB FDSOI technology [6]

Another benefit of this type of transistor structure, is the improvement of body biasing technique to modify its threshold voltage. It is possible to use forward body bias, FBB; and reverse body bias, RBB, to this UTBB FDSOI transistors.

Applying RBB, the transistor decrease the current leakage of transistor and increase the delay. It is useful to save energy, when the transistor has to work as a switch off or idle. For the NMOS transistor, RBB is in the range between 0 V and -300 mV; and for PMOS it is the same but with opposite sign, between 0 and 300mV.

Applying FBB, the transistor increases its working performance, but the leakage also increases. The use of forward body bias is used to achieve higher logic speed with lower voltage supply. In NMOS transistors, it is possible to use FBB up to 2 V or in the case of PMOS transistors, down to -2 V, achieving the benefits of this body biasing strategy [5]. Due to fabrication characteristics, the FBB cannot be higher than 3 V, which is the breakdown voltage.

LVT transistor are made to be used with FBB, where the benefits of tuning the threshold voltage are boosted. In Figure 8 simulation result of apply FBB to a LVT is shown, realizing that the NMOS transistors achieve better improvements in respect of PMOS. This simulation is made over PMOS and NMOS LVT transistors of 1 μm^2 and with a FBB up to ±1.2 V, that are the conditions the scope of this thesis.

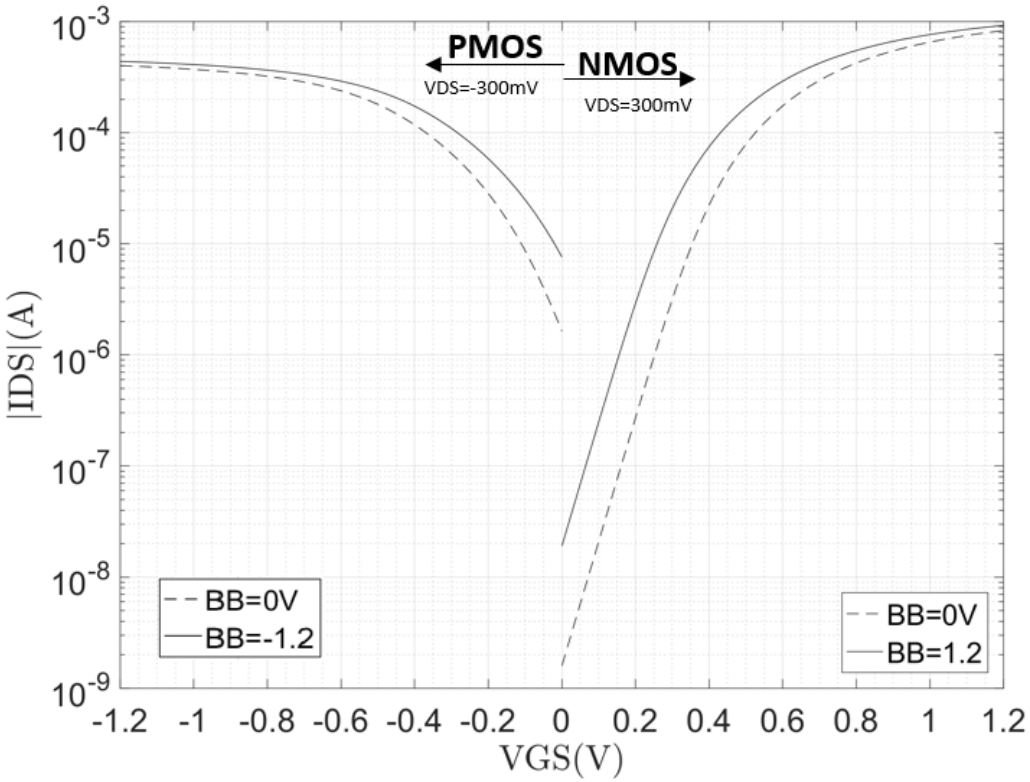

Figure 8. Behavior of LVT transistor with flipped well and ground plane of UTBB technology when FBB is applied.

4

CHARGE PUMPS: STATE OF ART

4.1. Introduction to Charge Pumps

In recent electronics circuits with lower voltage supply, V_{DD}, it is needed to achieve DC power converters that could generate output voltages, V_{OUT}, higher than V_{DD}. It is the case of some applications as SRAM, LCD drivers or RF antennas.

An electronic circuit that could be used to generate V_{OUT} several times higher than V_{DD}, is the Charge Pumps, CP. One of the principal characteristics of this type of converters is to use only switches and capacitors, avoiding the use of inductors; therefore it makes Charge Pumps very suitable to use in Integrated Circuits [15]. When voltage supply scales down with every technology node, CP are more and more used in all kind of circuits.

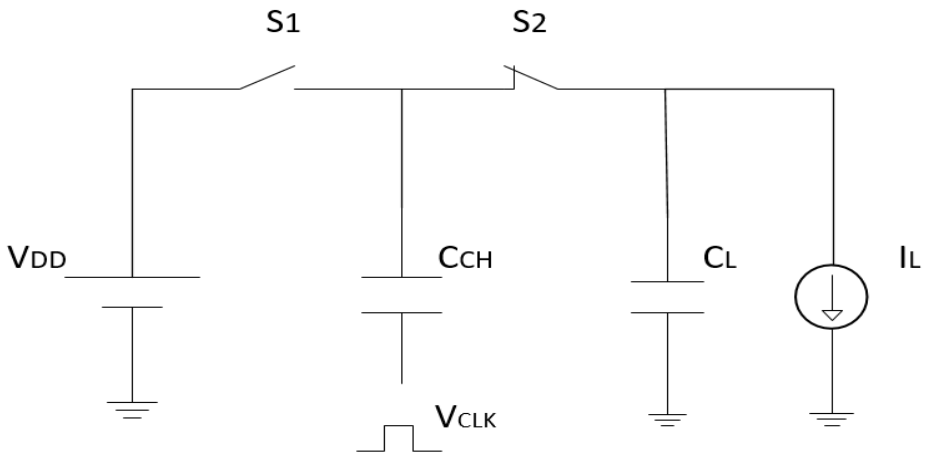

Figure 9. One stage Charge Pump

The basic structure of Charge Pump, only one stage, is shown in Figure 9. It is made up by one voltage supply, V_{DD}, two switches, S_1 and S_2, a capacitor to pump the charge, C_{CH}, a clock signal, V_{clk}, and an output load, that in this case is based in a current load, I_L, and a load capacitor, C_L. The amplitude of V_{CLK} has to be equal to V_{DD} and a stable period, T, where the ideal duty cycle is 50%.

The operation of the Charge Pump could be divided in two stages. In the first step, S1 is closed, S2 is opened and Vclk is in low level, 0 V. In this step the charge is transferred from the voltage supply to C_{CH}. In the second stage, S1 is opened, S2 is closed and V_{CLK} is in high level, V_{DD}. In this case, the charge stored in C_{CH} in the first stage is now transferred to the output. The operation of a single stage CP is shown in Figure 10.

In steady state, the output voltage reaches two times V_{DD} less the losses in the load, $\frac{I_L \cdot T}{C_{CH}}$. To achieve the output voltage of steady state, it is needed several clock's cycles, where in the first cycles the increment of V_{OUT} is very fast and when the output voltage is near to final value, the increment is slower. The generation is asymptotically to the steady state voltage.

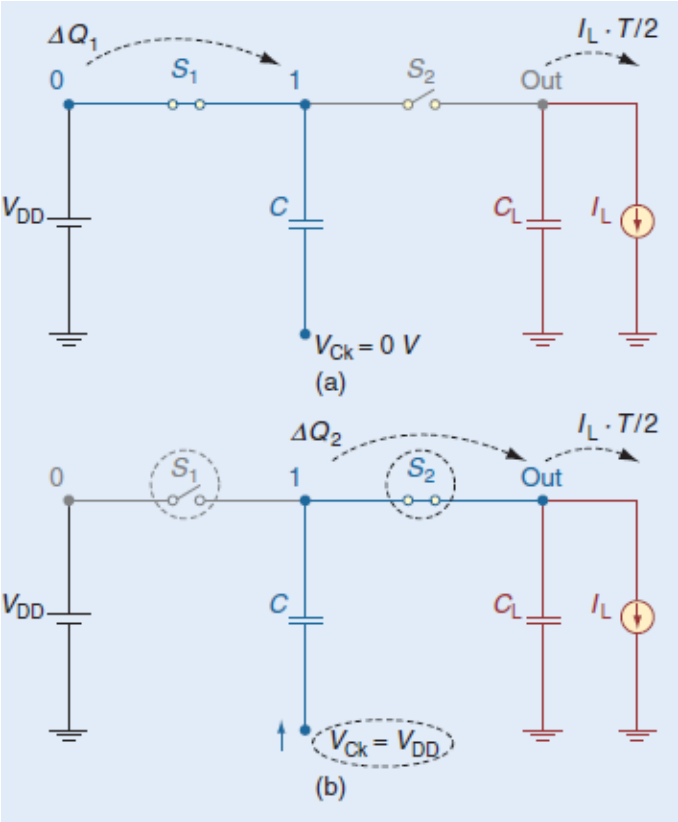

Figure 10. Basic operation of Charge Pump [15]

If output voltage is required to be higher than two times V_{DD}, several stages of Charge Pump can be connected in series. Each stage is based in one switch and one capacitor. The condition to achieve the transfer of charge between stages is that even and odd stages must get the clock signals in counter phase. If the Charge Pump has N stages, the output voltage is equal to

$$V_{out} = (N+1) \cdot V_{DD} - N \frac{I_L \cdot T}{C_{CH}}$$

Due to losses in the load, the output voltage has a ripple. The cause is that when the switch is closed, the voltage reaches the maximum value, but it decreases on time due to I_L. The output voltage ripple only depends on the load capacitor, assuming that C_L is higher than C_{CH}. It could be expressed as

$$V_{ripple} = \frac{I_L \cdot T}{C_L}$$

4.2. Principal parameters of Charge Pumps

To design a Charge Pump, some important parameters has to be studied. The most important are:

- Number of stages: depending on the output voltage required, the Charge Pump needs a specific number of stages, N. The ideal relationship between the number of stages, N, and the output voltage, V_{OUT}, is equal to

$$V_{out} = (N+1) \cdot V_{DD}$$

- Silicon Area: this parameter is important when the Charge Pump is implemented in an IC. The section of silicon needed by CP is mainly due to capacitors, then the area occupied could be estimated as

$$A_{TOTAL} = \mathcal{k} \cdot N \cdot C_{CH}$$

, where $\mathcal{k}$ is a parameter which depends on the process and technology used.
Another option to express the area is substituting C_{CH} in the V_{OUT} expression, resulting in the next equation

$$A_{TOTAL} = \mathcal{k} \frac{N^2}{(N+1) \cdot V_{DD} - V_{OUT}} \frac{I_L}{f}$$

Observing both equations, the area grows when the current of load increase or the frequency decrease. In fact, to provide more charge to the load, the capacitors C_{CH} has to be bigger.

- Current consumption: this parameter denotes the consumption of CP and it can be divided in two factors, I_{ideal} and I_{par} [16]. The first factor, I_{ideal}, is the consumption of ideal function of CP and it evaluated as transfer of charge to the load by the power supply through all stages. It could be represented as

$$I_{ideal} = (N+1) \cdot I_L$$

The Ipar denotes the current losses due to the parasitic capacitors and the switch time between transitions. To calculate these current losses, the effect of switching time could be neglected, remaining only the parasitic capacitors in a portion α of the total capacitance. I_{par} is expressed as

$$I_{par} = \alpha N C_{TOT} f V_{DD}$$

If both current factors are added, the current consumption is expressed as

$$I_{DD} = \left[(N+1) + \alpha \frac{N^2}{(N+1)V_{DD} - V_{OUT}} \cdot V_{DD} \right] \cdot I_L$$

Another two important parameters to analyze in the design of Charge Pumps with capacitive load are the followings

- Rise time: it is the time needed to reach the output voltage. As the load is purely capacitive, this time could be calculated as the time needed for a RC circuit, where the RC model of the Charge Pumps [17] could be shown as

$$R_{eq} = \frac{N}{C \cdot f}$$

- Charge consumption: in CP with purely capacitive load, this parameter is only calculated as the charge transferred by the power supply to the CP during the rise time. This consumption could be divided in the charge given by the load, Q_L, the charge required by C_{CH} during transient, Q_{pump}, and the charge wasted by the parasitic effects, Q_{par}. Then the total charge consumed is denoted as

$$Q_{TOTAL} = Q_L + Q_{pump} + Q_{par}$$

To optimize the design of Charge Pumps, different strategies could be adopted, depending on the requirements of the circuit. The two principal trends are to optimize the area or to optimize the power consumption. If the analysis of both strategies are compared, it exist an optimal point where both strategies could be possible, but out of this point, both strategies are not possible [15].

4.3. Different topologies of Charge Pump

In the last sections, Charge Pumps are analyzed with ideal switches. In this section, some of the principal structures of Charge Pumps are presented as the Dickson CP, Bootstrap CP, Double CP, Serial-Parallel CP or CP with adaptive number of stages. These topologies are explained in the next sub-sections.

4.3.1. Dickson Charge Pump

The first integration of CP was in 1976 by Dickson [18]. In this topology, the switches are done by diodes achieving the generation of voltage without any control signal; but in the other hand, the principal drawback is the losses of voltage due to the threshold voltage of the diode, more important in low voltages. With new silicon technologies, the diodes are replaced by MOS transistors, as it is shown in Figure 11.

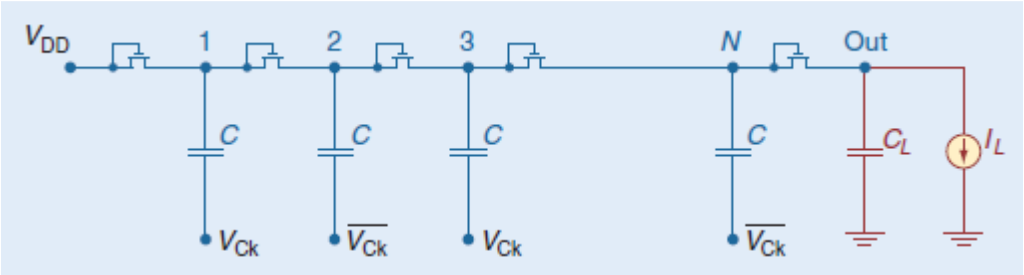

Figure 11. Dickson Charge Pump with MOSFET [15]

4.3.2.Bootstrap Charge Pump

Another variation for the switches of the Charge Pump is used in the Bootstrap CP [19] [20]. This structure is shown in Figure 12.

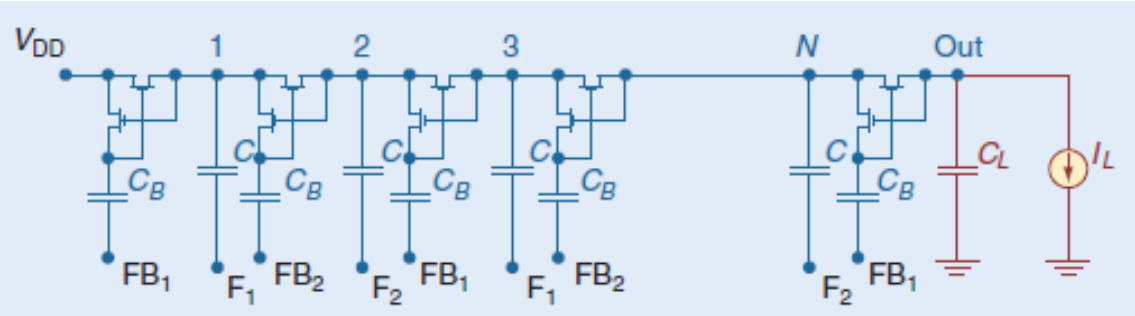

Figure 12. Bootstrap Charge Pump [15]

In this topology, the switch is auto controlled, but it needs an extra capacitor, denoted C_B, to charge the voltage between half of a period of the clock. It also has the drawback that the required clock is more complex, requiring four phases and $2 \cdot V_{DD}$ of amplitude. It is shown in Figure 13.

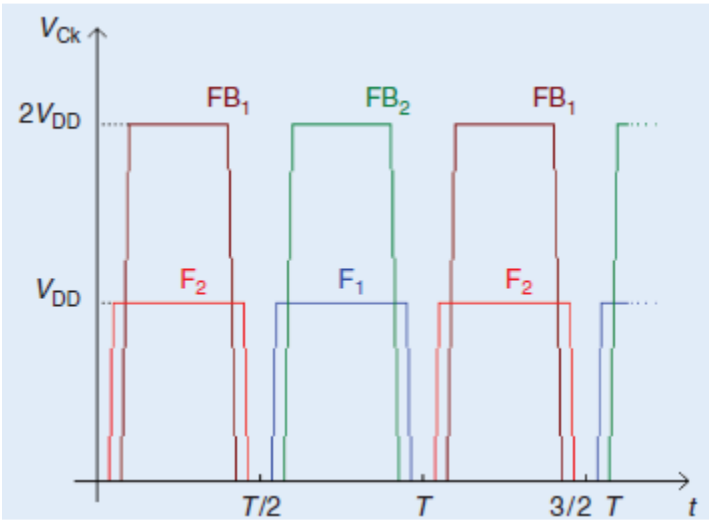

Figure 13. Clock Signals for Bootstrap Charge Pump [15]

4.3.3.Double Charge Pump

The Double Charge Pump is a topology designed to reduce the ripple of the output voltage. This structure is bases in create two complementary CP with the half of the capacitors C_{CH} of the Dickson CP, providing each CP the charge to the load in every half of period. The output voltage obtained is the same, but the ripple is

$$V_{ripple} = \frac{I_L \cdot T}{2 \cdot C_L}$$

, the half of the other CP. The basic structure of Double CP is shown in Figure 14, but it allows the implementation of Dickson or Bootstrap CP topologies.

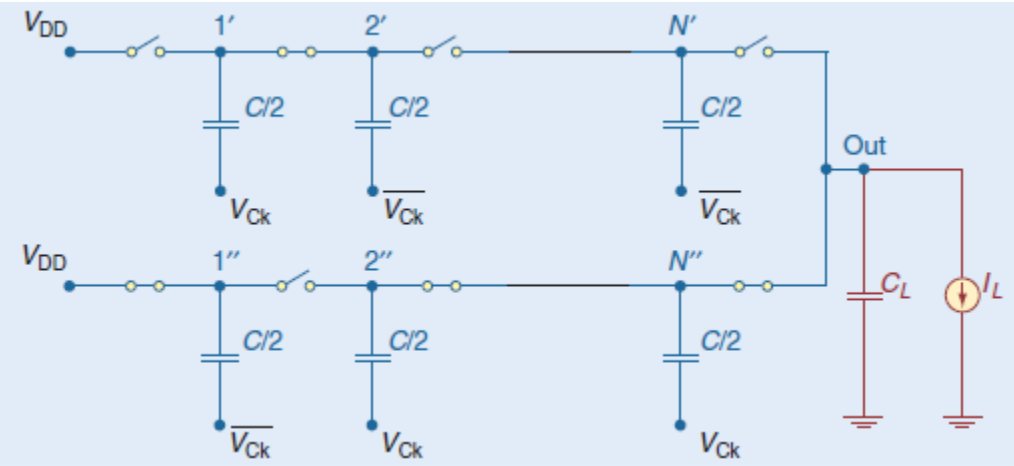

Figure 14. Double Charge Pump topology [15]

One variation of this topology is the Latched Charge Pump [21] [22], also known as Gate Cross-Coupled Charge Pump. This variation is suitable for very high clock frequencies. Another advantage respect to Bootstrap CP is that it only need one clock signal with two phases and an amplitude V_{DD}. This is the topology used for the design of this thesis.

4.3.4.Series-Parallel Charge Pump

The Series-Parallel Charge Pump has the characteristic that all the capacitors are charged in the first half of period, where switches P_i and $P_{'i}$ are closed and switches S_i are opened. In the second half, the switches change its position and the charge is transferred to the output load. The main drawbacks are due to parasitic capacitances, that decreases its performance, and the implementation of switches. This topology is not very used in IC by its inefficiency. In Figure 15, two stages of this CP structure is shown.

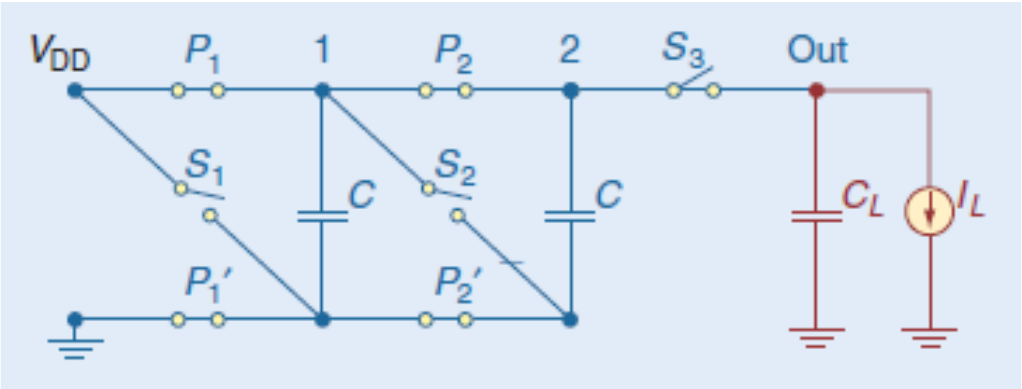

Figure 15. Two stages of Series-Parallel Charge Pump [15]

4.3.5.Charge Pump with adaptive number of stages

Charge Pump with adaptive number of stages top is used in IC designs which require different output voltages generated by variable number of stages. The control of number of stages of CP are dynamically adapted with the requirements of design. One example of this CP topology is shown in Figure 16 [13].

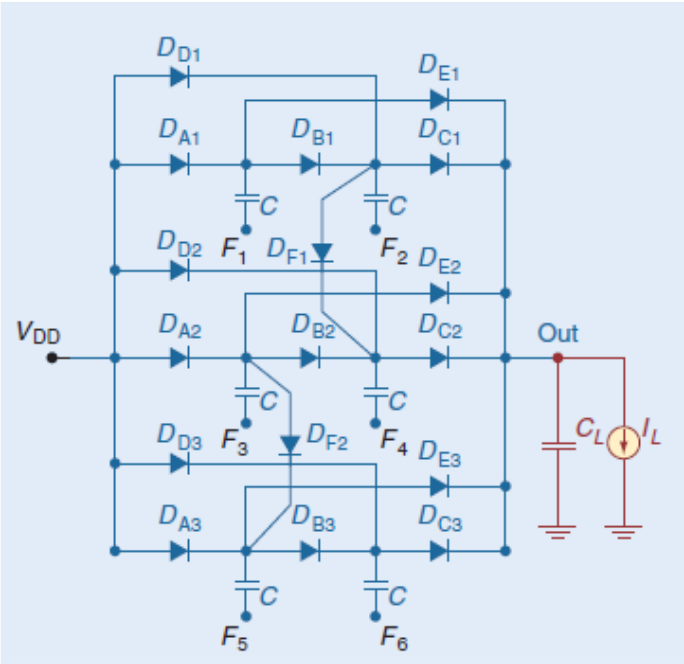

Figure 16. Charge Pump with adaptive stages [15]

5

DESIGN OF BODY BIAS GENERATOR

5.1. Introduction

The objective of this chapter is to describe design of a Body Bias Generator, BBG, to improve application circuits based on UTBB FDSOI of 28 nm. Along this chapter, the architecture of BBG is presented, also is explained more in detail the design of each block. When all blocks are designed, the simulation of BBG is shown in different cases of FBB. Finally, the optimization of the circuit is described and the results are show.

5.2. Architecture of Body Bias Generator

The objective of Body Bias Generator is to design a voltage generator from a voltage supply of V_{DD} of 300 mV. It shall provide at least ± 1 V to be used as Forward Body Bias for NMOS and PMOS.

This block should be applied to application circuits for improving their performance when it is required. For this purpose, the BBG shall be controlled by an enabling signal to generate or not the voltage, allowing the reduction of power consumption when the circuit is in idle mode or switched off. Figure 17 shows the variation of current when body bias is applied to MOSFET in the range of voltage supply of 300 mV.

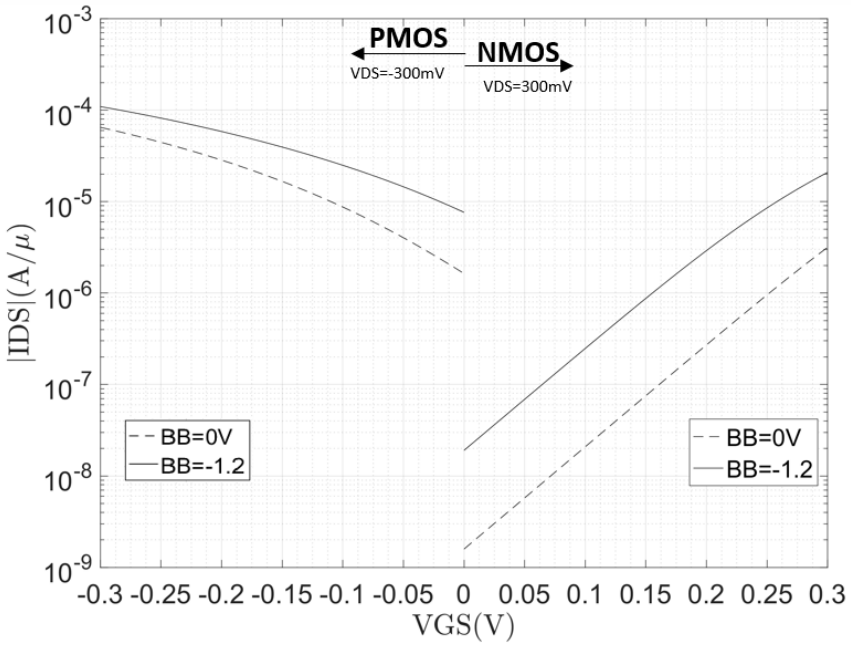

Figure 17. LVT UTBB FDSOI 28 nm behavior

With the characteristics and functions of BBG, the interaction with external components is resumed in Figure 18, which shows the black box diagram of BBG and the interconnection with the application circuit. The input signal is the enable_BBG and the outputs are the voltage of Body Bias, positive for BBnmos and negative for BBpmos. The voltage supply is 300 mV.

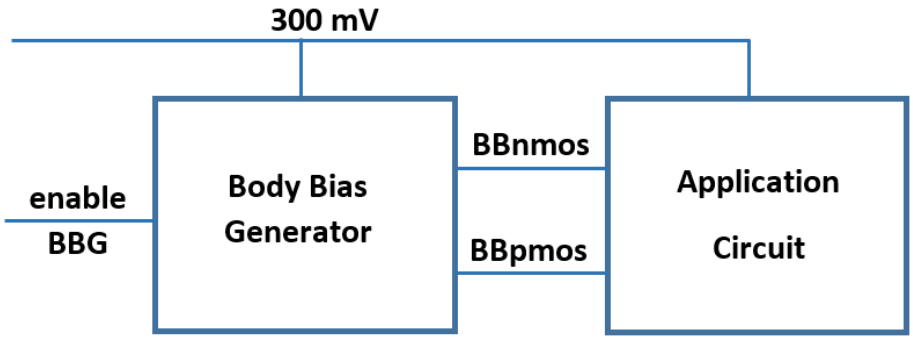

Figure 18. Black box diagram of Body Bias Generator [6]

For the design of BBG, a charge pump is used to generate the higher positive voltage, specifically the Gate Cross-Coupled Charge Pump, GCCCP. To be work properly, when the GCCCP has more than one stage, it is needed to use a clock signal of amplitude VDD and with two phases. To provide the clock signal, it is designed a Ring Oscillator, RO, and then this signal pass through the Non Overlapped Clock, NOC, to create both phases. Finally, a Negative Charge Pump, NCP, is used to generate the negative voltage. In Figure 19 is shown the architecture of the Body Bias Generator with the main blocks and its interconnection. In the next section, the design of all blocks are shown and this function is explained more in detail.

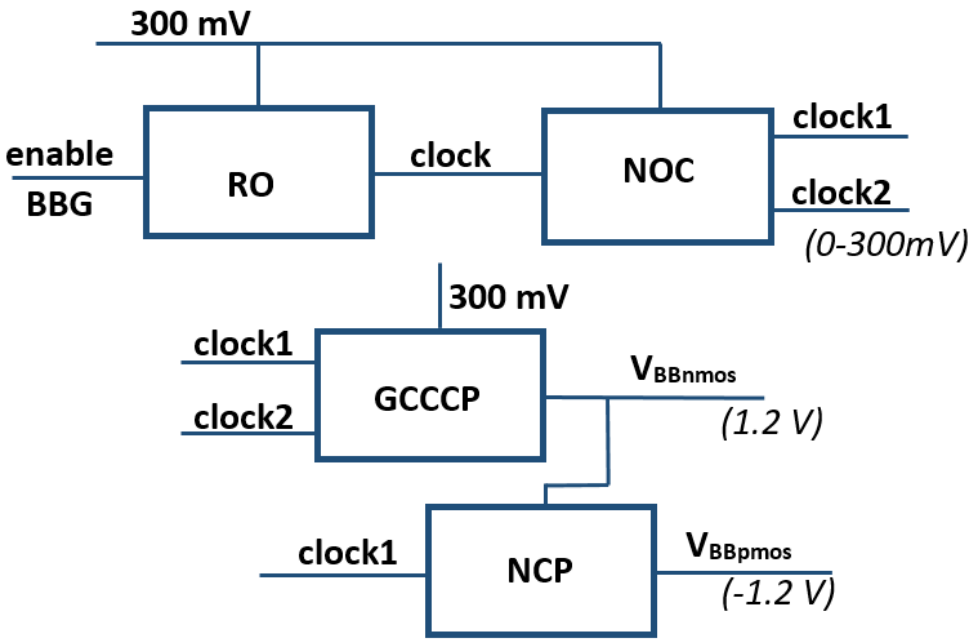

Figure 19. Architecture of Body Bias Generator [6]

5.3. Design of Body Bias Generator

In this section all the blocks that be part of the Body Bias Generator are designed and its function is explained more in detail. The objective of this block, as it was explained before, is to generate at least ±1 V. The order of the section is to explain the electrical model designed in sequential order from the control signal enable_BBG, it means, first the RO, then the NOC to explain the generation of the clock signal with two phases, next the GCCCP that uses this clock signal to generate the positive voltage and finally the NCP which provides a negative voltage from the output voltage of the GCCCP.

5.3.1.Ring Oscillator

The Ring Oscillator is an electronic circuit made by an odd number of inverters to create a clock signal. The basic structure of RO is shown in Figure 20.In this case the first inverter is substituted by a NAND gate to control the generation of the clock signal, therefore the generation of voltage is stopped. This structure of clock generation is very useful for Integrated Circuits because it only need basic logic gates, inverters and NAND if a control signal is needed.

The frequency of the clock signal depends on the number of stages of inverters as well as the performance of inverter gates. The period of the signal depends on the rise and falling time of the signals on the inverters, propagating this delay in each stage. If it used faster transistors, faster are transitions between logic levels and in consequence, frequency of clock is higher.

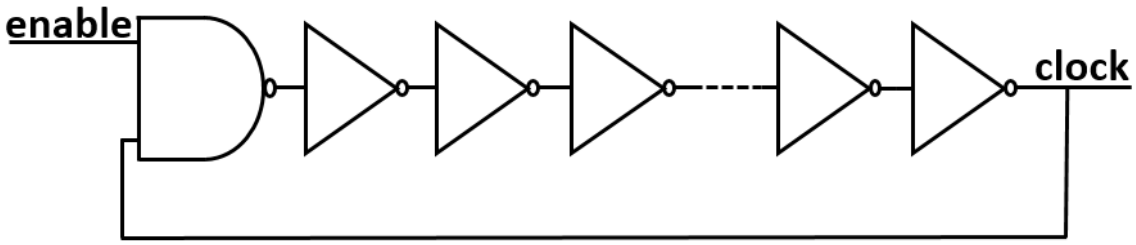

Figure 20. Structure of Ring Oscillator [6]

It is also important in the design of RO that the clock signal has a duty cycle of 50% or the closest possible. If denotes the time that switch of charge pump is opened or closed. Another factor to take into account with the clock signal is to achieve that rising and falling time are the lower possible, to achieve the faster switching and low current losses in transitions.

An important remark about the Ring Oscillator is that in this circuit never has to be applied FBB feedback, because it makes the clock's frequency increases and it modifies the operation of BBG, due to the relationship between the capacitors and the frequency.

5.3.2.Non-overlapped dual-phase clock

Once the clock signal is providing by RO, the next step is use the non-overlapped dual-phase clock, NOC. It is the circuit that can generate the two phases of the same clock, used by Gate-Cross-Coupled Charge Pump, explained in the next subsection.

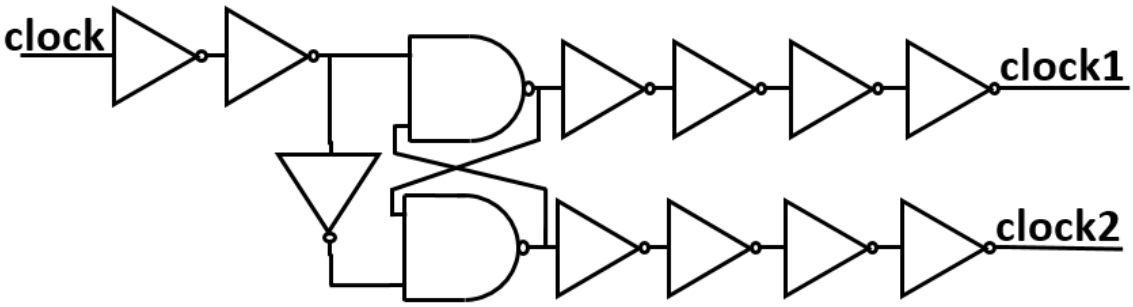

Figure 21. Structure of non-overlapped dual-phase clock signal [6]

In Figure 21 is observed the structure of NOC. In this model, the first inverter gates, known as drivers, are used to provide to clock signal the required charge demanded by the circuit. It is needed to remain the signal identical to the output of RO, accomplish the requirements of the signal. The same is for the inverter gates of output, which works also as drivers.

The clock signals generated by this block, has to be in counter phase in each output. It means that when clock1 is in high level, clock2 is in low level. The ideal behavior of both signals is to that the transition are synchronized, starting at the same time and having the same rise and falling time. If it is achieved, the ideal cross point of transitions is in $V_{DD}/2$. If it is possible, the switches of Charge Pump are synchronized and when one is opened, the complementary switch is closed, avoiding losses in each stage.

As ideal case is very difficult, it is important to avoid that complementary switches of GCCCP are opened at the same time, preventing the losses of charge. To assure that this situation doesn't occurs, the NOC generates both clock signals in counter phase, as is shown in Figure 22. Where both signals are in the same level, low level, during transitions, switches of GCCCP are closed. This solution makes that charge period are not the ideal, but prevent it for higher losses when complementary switches are opened at same time.

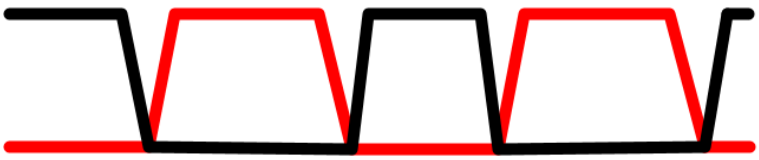

Figure 22. Non-overlapping dual-phased clock

To reduce the time when both clock signals are in the same level, it is important to achieve that NAND gates and the inverter gate that is connected to bot NAND are the faster possible.

5.3.3.Gate-Cross-Coupled Charge Pump

To generate positive voltage of Body Bias Generator, the topology of Gate-Cross-Coupled Charge Pump. The structure of GCCCP is shown in Figure 23. In this topology is used 4 transistors by stage, two NMOS and two PMOS.

As is explained in Chapter 4, the ideal output voltage of a Charge Pump is calculated as

$$V_{OUT} = (N + 1) \cdot V_{DD}$$

, where N is the number of stages. In this case, as the BBG shall provide at least 1 V and the supply voltage is 300 mV, used in V_{IN} and the clock signals, the minimum number of stages needed are three. With this configuration, the ideal output voltage is 1.2 V.

With this topology, every stage can be divided in two parts, top and bottom part. Both parts have different clocks in counter phase, generated by the NOC. To explain the basic operation of GCCCP, top part is used. When the clock1 has low level, 0 V, M1 is opened to charge the capacitor C_{CH} and M3 is closed. When the clock has high level V_{DD}, M1 is switched off and the M3 is opened, transferring the charge to the next stage or the load in case of the last stage. Bottom part works in the complementary manner, when top is charging phase, bottom is in transfer phase and vice versa.

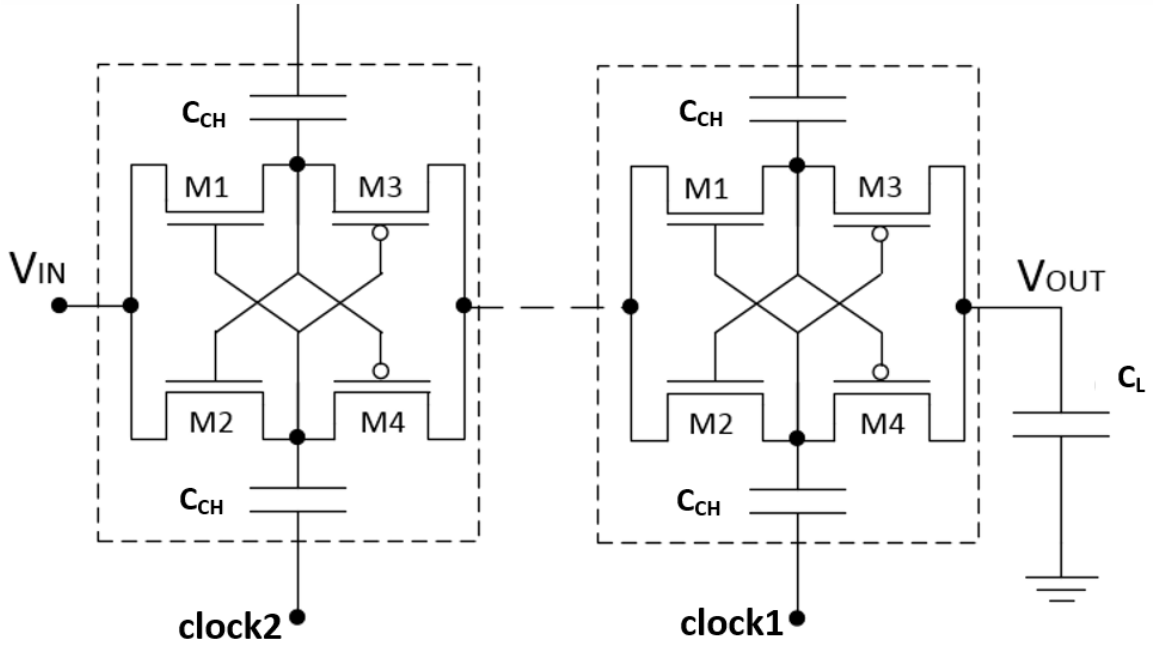

Figure 23. Structure of Gate-Cross-Coupled Charge Pump [6]

Knowing the functioning of GCCCP, it explain the importance of the clock generation of two phases, to avoid that when some part is in transfer mode, the complementary part has the PMOS closed, avoiding the transfer of charge from both parts. It could be reflected is voltage losses in every stage.

Another important factor when the GCCCP is designed is the sizes of capacitors. Capacitors are the principal factor of area, determining the circuit's size. Capacitors C_{CH} are also important to generate the output voltage, as it explained in Chapter 4 and it is expressed like

$$V_{out} = (N+1) \cdot V_{DD} - N\frac{I_L \cdot T}{C_{CH}}$$

, that is the real value of the output voltage, taking into account losses. In the case of C_L affects the ripple of V_{OUT} as is shown in the next equation

$$V_{ripple} = \frac{I_L \cdot T}{C_L}$$

5.3.4.Negative Charge Pump

To use the Body Bias Generator as a voltage source to apply in Forward Body Bias techniques, it is required that negative voltage is also generated. In Figure 24 is shown the structure of Negative Charge Pump composed of Level Shifter, LS, and a special stage of the Gate-Cross-Coupled Charge Pump.

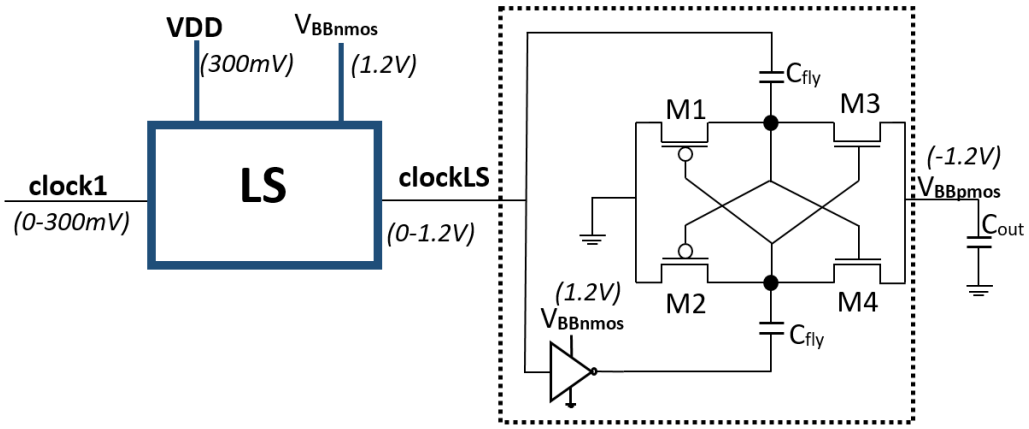

Figure 24. Structure of Negative Charge Pump [6]

In the case of the topology of Charge Pump, it is possible to observe that the CP has a similar structure of one stage of GCCCP but with the PMOS and NMOS interchanged. Another difference is that input voltage this time is the ground, 0 V, and the clocks have an amplitude equal to the value generated in GCCCP, in the ideal case is 1.2 V. In this case, the output voltage can be calculated as

$$V_{OUT} = V_{IN} - N \cdot V_{DD}$$

, where in this case the VIN is 0 V, VDD is 1.2 V and it only has one stage.

How it is explained for the GCCCP, one important factor for the capacitors, C_{fly} and C_{OUT}. In this case, the losses in the output voltage are less dependent in relation with the capacitor C_{fly}, because the design only have one stage. It means that the C_{fly} could be smaller than C_{CH} to have the same losses.

In the case of the clock, in this cases the two phases are generated by an inverter gate. It is due to the voltage supply of the inverter, provided by the BB of NMOS, is 1.2 V, further than the threshold voltage, improving the speed of this component and in consequence the counter phase has faster transitions.

5.3.4.1. Level shifter

The Level Shifter is used to generate a clock signal of the same amplitude of the voltage generated in the GCCCP, enabling its use for the NCP. In Figure 25 is shown the structure of the Level Shifter.

The topology of the LS is based in a cascode topology. This type of circuit has the benefit that it has high slew rate, then it could be capable to follow faster signals. This characteristic is important, because the signal that LS has to adapt the voltage is the clock signal, with frequency of some tens of MHz. With voltage supply of 300 mV or less in the first steps of

the GCCCP, the gate delay is high, worsen the clock signal generated, therefore the negative voltage generated is worst, then it is important to preserve the quality of the clock signal in these first steps of generation.

Another factor to take account when the circuit is designed, is voltage supply of each inverter gate. In the case of bottom inverter gate, it is used to change the level of the clock signal from NOC with an amplitude of 300 mV, then its voltage supply has to be 300 mV. The output's inverter gates are used as drivers for the output clock signal, that has an amplitude of V_{BBnmos}, in the ideal case, then the voltage supply for these inverter gates shall be V_{BBnmos}.

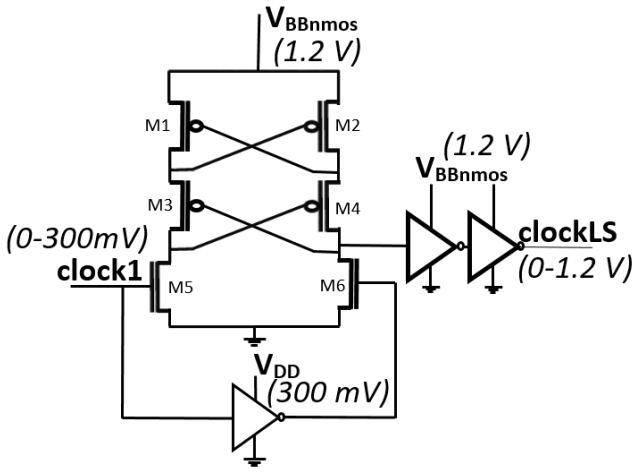

Figure 25. Structure of Level Shifter [6]

5.4. Simulation of Body Bias Generator

To simulate the BBG electrical model, it is used the simulation tool of Cadence. The voltage supply used is 300 mV, the same as in the requirements. The input signal of control, enable_BBG is in high level all time, to allow the generation of body bias.

In this simulation, several metrics are used to measure the quality of the circuit. The metrics analyzed are:

- Steady state voltages (SSV) of BBnmos and BBpmos, that are the final values of voltages obtained when it is stabilized in the time.
- Setting time of BBnmos and BBpmos, which are the time needed to achieve the 90% of the SSV until the start of generation of voltage.
- Overall power consumption that is the total power consumption of all the components of BBG.

Also to evaluate the effect of the FBB in the performance of the electronics designs, three cases are simulated:

1. BBG without FBB feedback
2. BBG with FBB feedback in NOC block
3. BBG with FBB feedback in NOC and GCCCP.

In the simulation the values of the capacitances are 300 fF for C_{fly} and 1pF for C_{CH} and C_L. The frequency of the clock is 30 MHz.

5.4.1.BBG without FBB feedback

In this case, the BBG doesn't use any FBB feedback for its blocks. The first signal to analyze is the clock signal with two phases in the output of the NOC, shown in Figure 26. Observing the signal, it is possible realize that signal are not completely overlapped and this rise and falling transitions are slower.

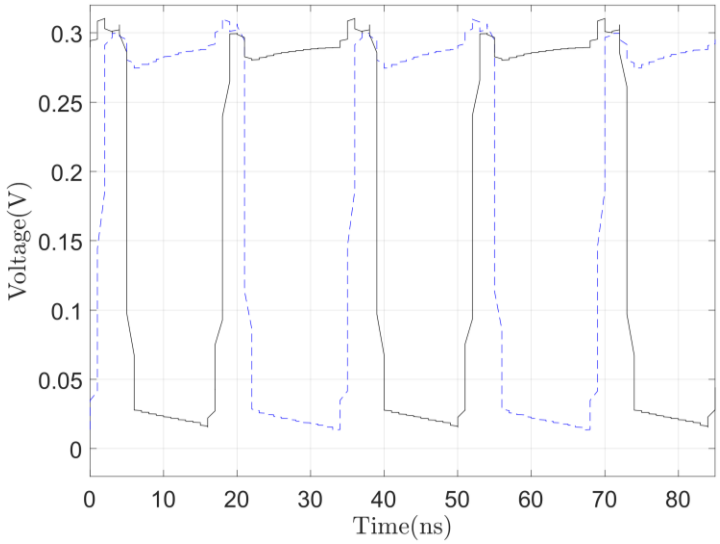

Figure 26. Clock signal with two phases of BBG without FBB feedback

In consequence of these degraded clock signals, the SSV of BBG are low. The cause is the high switching losses. In Figure 27 is shown the output voltages of BBG and the SSV values are far than the ideal output voltage of 1.2 V.

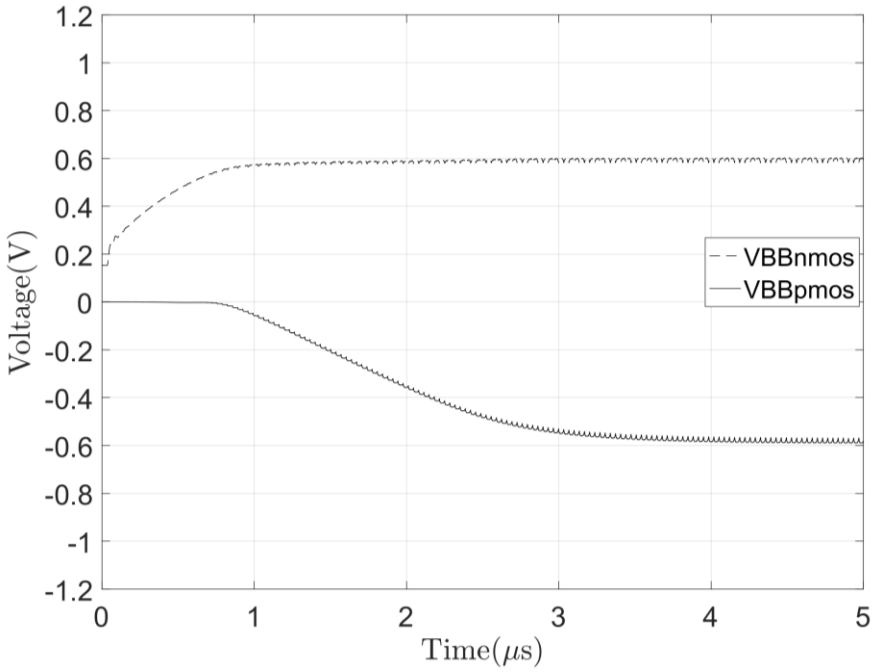

Figure 27. Output voltages of Body Bias Generator without FBB feedback

5.4.2.BBG with FBB feedback in NOC

In this case, the simulation is the same that in the previous case. The only difference in that this time, the block non-overlapped dual-phase clock, NOC, has FBB directly from the output of CP. In this case, the clock signals generated are better, as it is shown in Figure 28. As it is observed, with the FBB in the NOC, the clock signal is practically non-overlapped and the rise and falling transition are faster, enabling a better switching in the GCCCP.

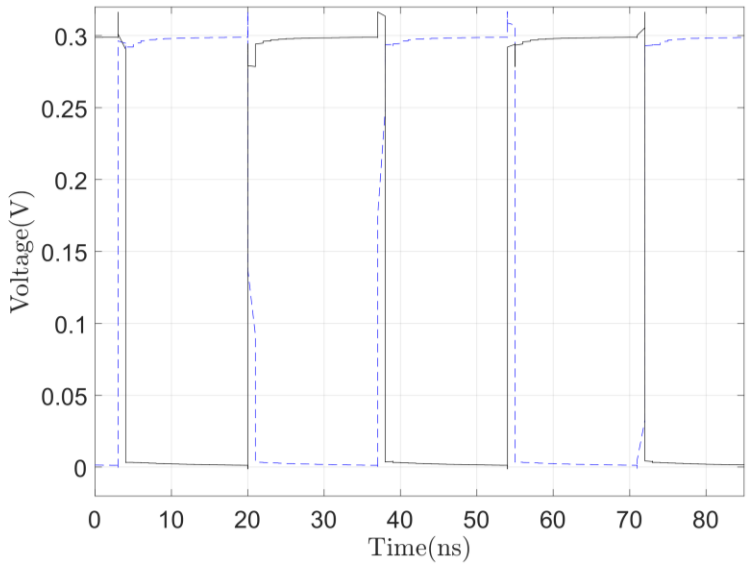

Figure 28. Clock signal with two phases of BBG with FBB feedback in NOC

In Figure 29, it is possible to observe how the voltage generation increases, reaching values over ±1V. This is only due to a better clock signal, enabling a better switching of CP and reducing the losses between transitions. This case emphasizes the importance in the quality of the clock signal with non-overlapped phases and faster transitions between low and high level.

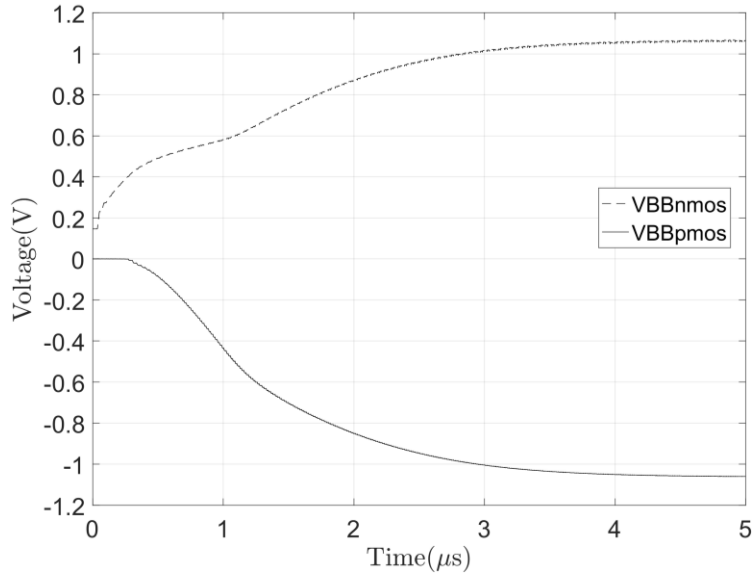

Figure 29. Output voltages of Body Bias Generator with FBB feedback in NOC

5.4.3.BBG with FBB feedback in NOC and GCCCP

For this simulation, the FBB generated by the BBG feedback the NOC and GCCCP blocks. In Figure 30 is shown the clock signals in the output of NOC. In this case, it possible to realize that the clocks are very similar that in the case of FBB feedback in NOC, but in high level, V_{DD}, or in low level, 0 V, the signals do not reach the final value immediately. The reason is that now, the GCCCP block is also allow higher current flows through the transistors, NMOS and PMOS, demanding higher values of current when the capacitors, C_{CH} are in charge phase.

In Figure 31, the simulation of output voltages are shown. In this case, the steady state is a bit higher than in case of FBB feedback in NOC, but the difference more notable is speed to reach the steady state. It is caused by the same reason that is explained before for the modification of the clock signal. When the FBB is applied to the transistor of GCCCP the charge allowed to pass through it is higher, as is shown in Figure 7. It means that the charge of capacitor in each half of clock period is higher, transferring more voltage in first steps.

In the other hand, the increase of current by the FBB has a drawback, because it also increase the losses of the design. These losses are produced by the current leakage, higher than in the case without FBB, and the switching losses.

To solve the first cause, it is needed to design a circuit that applies the FBB only when the transistor is in conduction. This solution is out of the scope of this thesis. To solve the second cause, it is important generate a clock signal with dual phase the most similar to the ideal, perfect complementary signals and instantaneous transitions between high and low level. This solution is proposed in Section 5.5.

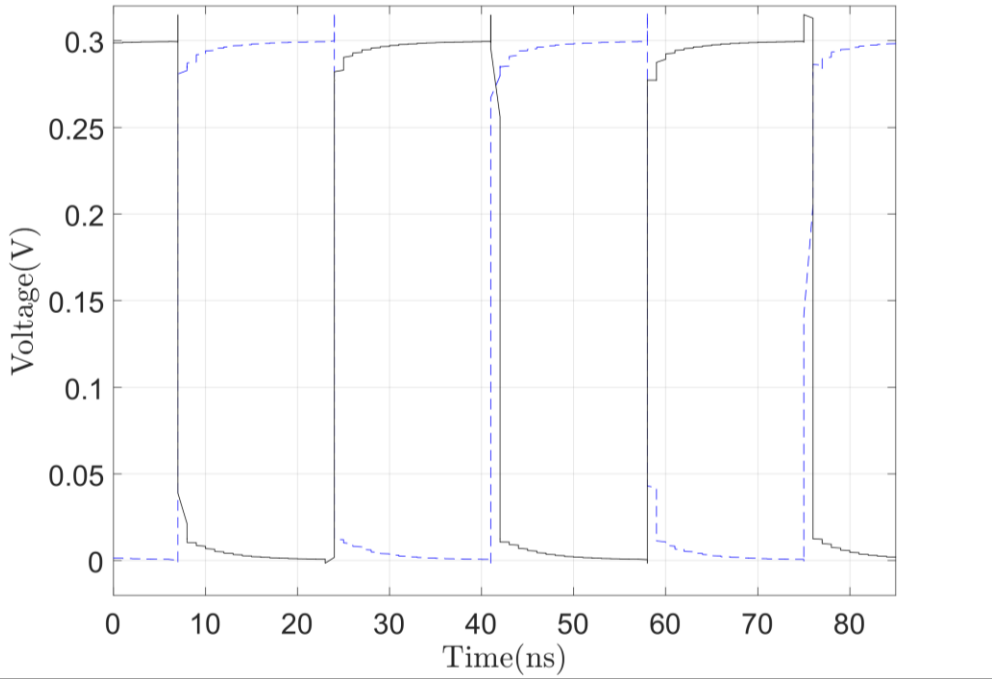

Figure 30. Clock signal with two phases of BBG with FBB feedback in NOC and GCCCP

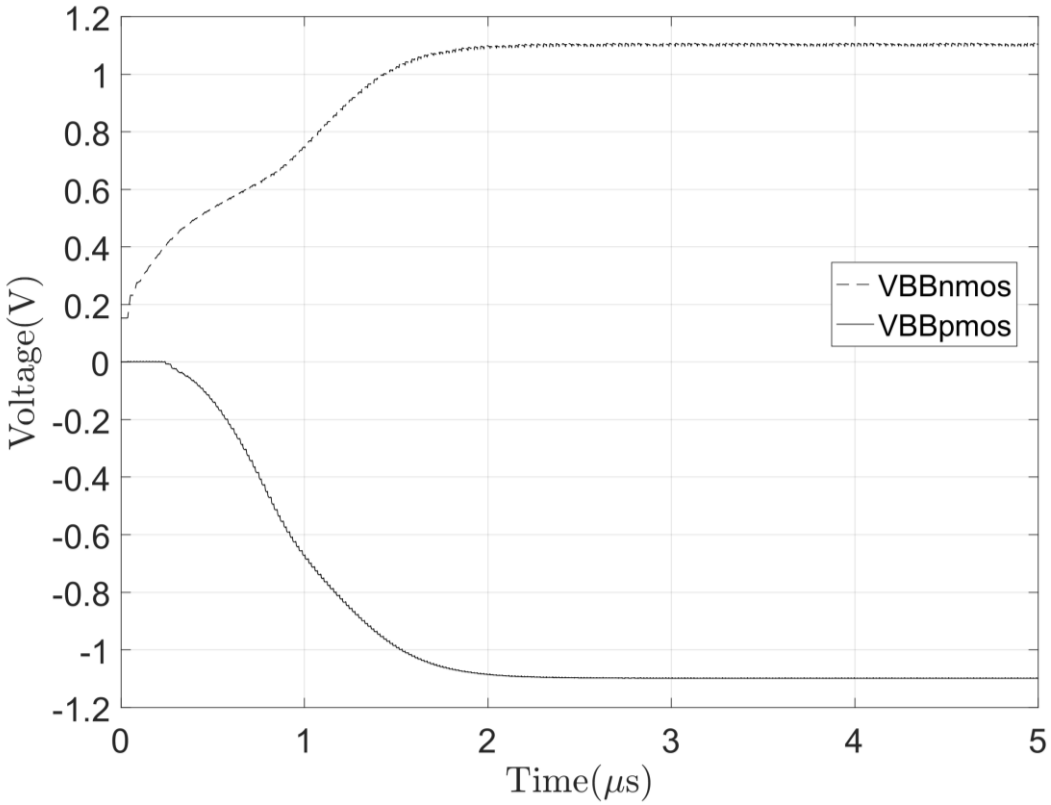

Figure 31. Output voltages of Body Bias Generator with FBB feedback in NOC and GCCCP

5.4.4. Analysis of simulation and results

In the simulation, the importance of the quality of clock generation is emphasize. Only with an improvement on the clock signal, with FBB feedback in NOC, the voltage generation increase, being closer to the ideal value of CP.

In the voltage generation, it is possible to observe a pattern in the positive voltage, BB of NMOS, and in the negative voltage, BB of PMOS. When the BBG starts, the positive voltage starts to increase immediately in an exponential way, but the negative voltage does not increase until the positive voltage reach the voltage that can create the correct clock signal for the NCP.

When the NCP starts to generate the negative voltage, the positive rise slowly. It is due to NCP charge is power supplied by the positive voltage, demanding more current than the load capacitance. Once both voltages has a similar amplitude, one positive and other negative, the increase again in an exponential way until the steady state voltage, SSV. The voltage generation of the BBG responds to a capacitor charge, due to the behavior of CP.

Respect to SSV, the voltage generated by the positive CP is always equal or higher than negative voltage, due to the losses in the NCP and in LS.

In the Table I is shown the metrics of each case. As it is observed in the simulations and the SSV are better when the FBB feedback is applied to NOC and GCCCP. Another metric that was analyzed before is the setting time, which is also better when FBB is applied to NOC and GCCCP.

Table I. Results of simulation of the Body Bias Generator

Metric	Without FBB	FBB in NOC	FBB in NOC and GCCP
SSV (BB NMOS)	590 mV	1.06 V	1.10 V
SSV (BB PMOS)	-580 mV	-1.06 V	-1.10 V
Setting Time (BB NMOS)	695 ns	2.49 µs	1.42 µs
Setting Time (BB PMOS)	2.73 µs	2.57 µs	1.51 µs
Power Consumption	2.997 µW	2.400 µW	3.178 µW

Respect of the overall power consumption, it is possible to observe that the values obtained, the better power consumption is obtained when the FBB feedback is only in the NOC. Here, it is possible to observe the relationship between power consumption and the voltage generated. If the voltage generation needs higher performance, higher voltage and faster generation, the power consumption also increase.

5.5. Optimization of Body Bias Generator

In the simulation of the Body Bias Generator, the objective of the voltage generation was achieved, providing voltage higher than ±1 V. But in the case of the power consumption, the results was further of the goal of the design, less than 1 µW of consumption.

In this Section, the optimization process of the BBG is explained. The optimization factors to take into account in this thesis are the power consumption and the area required by the circuit to create a BBG that accomplish all the objectives proposed.

First of all, the design is focused on achieving a BBG that could achieve the voltage generation of ±1V with a power consumption lower than 1 µW. The first element to analyze is the frequency of the clock generated by RO. In this case, ideal clocks are used to simulate the circuit and analyze how affects the frequency to the power consumption and the voltage generated, focusing in negative voltage, that it has always equal or lower amplitude than the positive voltage.

In Figure 32 is shown the simulation of BBG, where the power consumption is analyzed in function of the frequency of the clock and the capacitor C_{CH} of the GCCCP. In this simulation the C_{fly} is 300 fF and the C_L is 1pF, as in the simulation of Section 5.4.

Observing the results, it is possible to establish that the power consumption of the circuit depends on the frequency of the clock, obtaining a great power reduction if the correct value is selected. In the simulation it is also important to observe, how the value of the C_{CH} it is also important in the power consumption of the BBG.

Another relationship is the voltage generated with the clock's frequency and C_{CH}. If the clock's frequency is higher, the negative voltage is worst. In the case of $C_{CH,}$ it works in the contrary manner, if the CCH is lower, the negative voltage is worst. These considerations are important to achieve the generation of ±1 V by the BBG.

In this case, to achieve both objectives, generation of ±1 V with a power consumption lower than 1 μW, the initial conditions for the optimization are:

- Clock's frequency between 10 MHz and 20 MHz,
- CCH has to be higher than 300fF
- Cfly between 200 fF and 400 fF

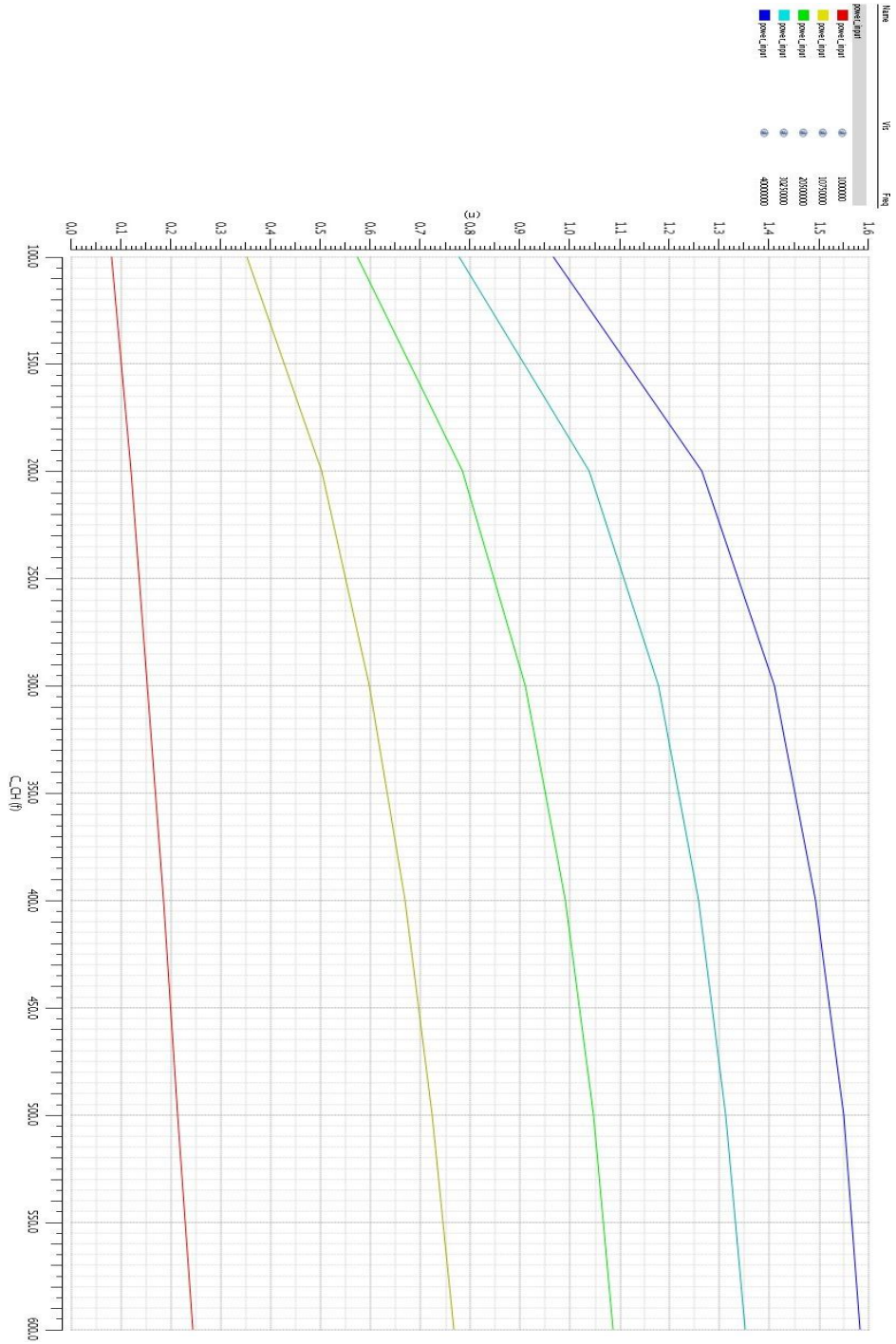

Figure 32. Analysis of Power Consumption vs Clock's frequency and CP capacitor

When the optimal frequency is selected for lowest power consumption, it is needed to create a RO with the best quality of clock signal. It is possible resizing the inverter gates of the clock and selecting the number of stages needed. For this design, the optimal clock generated is 14.5 MHz and it has to be fix, it means, the RO never has to use the FBB for its logic gates.

The next step is to optimize the NOC to obtain a non-overlapped dual-phase clock to be used by the GCCCP and the NCP. It is important to design good drivers, to provide the enough current to all the CP, without any loss of quality of the clock signals.

Once the optimal clock is created, the next step is to modify all the other blocks to generate the higher voltage possible for this frequency. To improve the generation, all the transistors have to be resized and the FBB has to be applied to the components that needs more capacity to transfer charge.

When the voltage generation and the power consumption are done, the optimization of the area is also possible. To do that, the values of the capacitors of GCCCP and NCP shall be reduced, therefore the area needed to implement them are smaller. As it is explained in Section 4.2, capacitors are the main contributors to the area in CP circuits.

To compare the improvements on the circuit, the same simulations of the Section 5.4 are done. The value of the capacitors are 1 pF for C_{CH} and C_L and 300 fF for C_{fly}. For the simulation, the FBB feedback is done in the same blocks as the section and in the same way.

5.5.1. Optimized BBG without FBB feedback

In Figure 33 is shown the clock signal in the output of NOC, where the quality of the signal is improve respect to the same signal before the optimization. In Figure 34 the simulation of the voltage generation is represented, realizing the higher voltage generated.

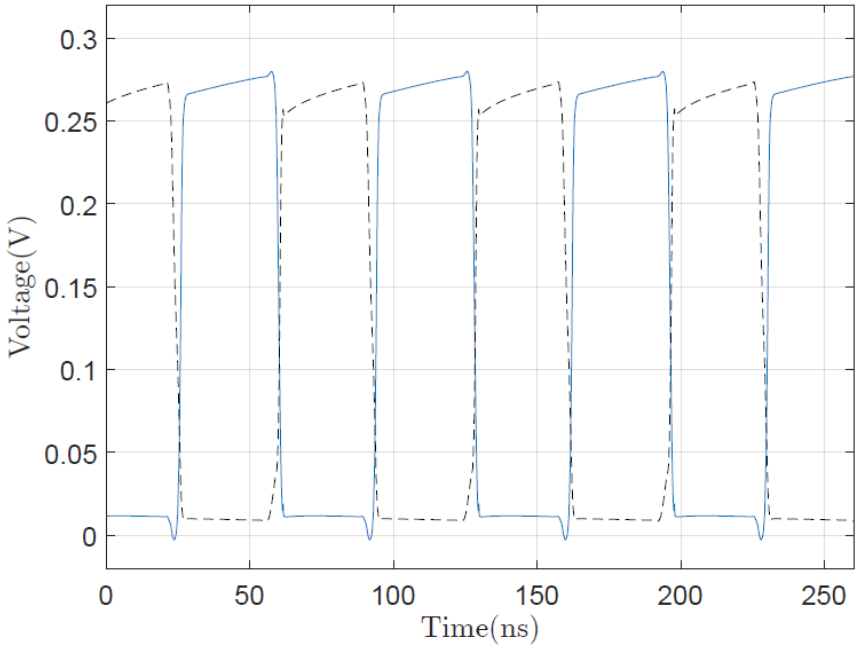

Figure 33. Clock signal with two phases of Optimized BBG without FBB feedback

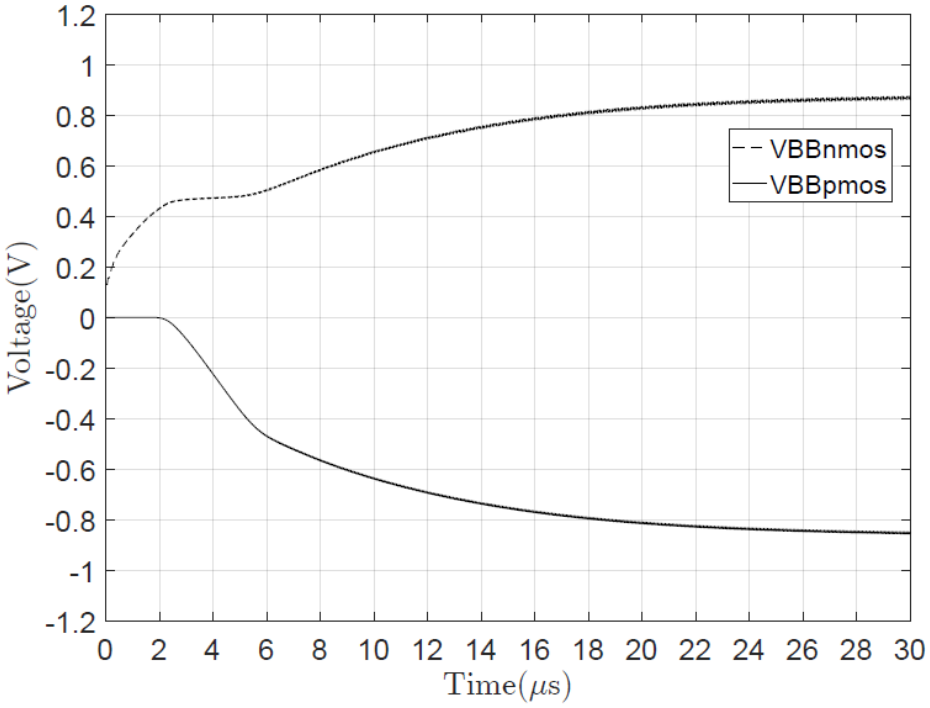

Figure 34. Output voltages of Optimized BBG without FBB feedback

5.5.2.Optimized BBG with FBB feedback in NOC

The simulation of clocks in the output of NOC is shown in Figure 35 and the output voltages in Figure 36. With the feedback in the NOC, the clock signal is very similar to the ideal one.

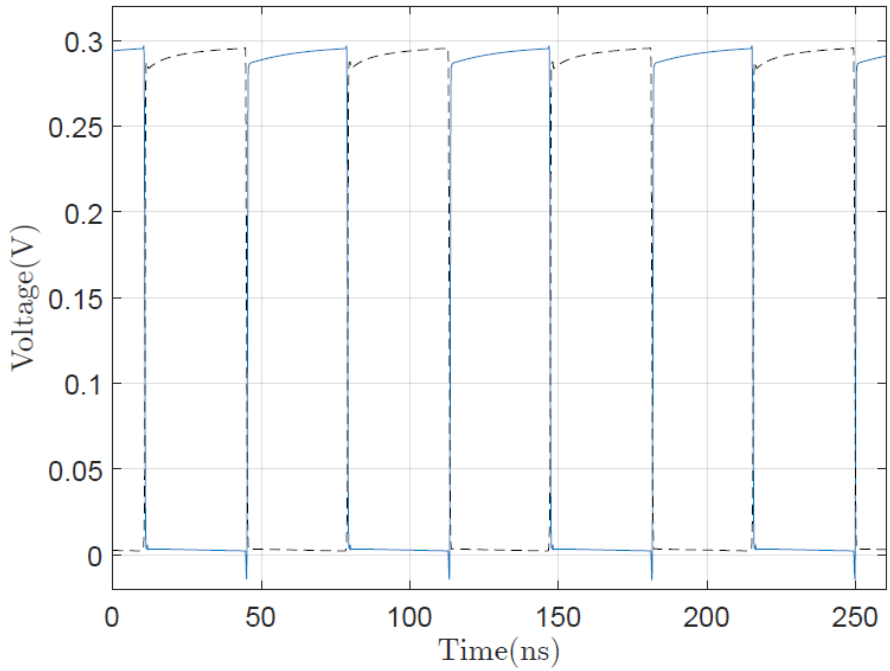

Figure 35. Clock signal with two phases of Optimized BBG with FBB feedback in NOC

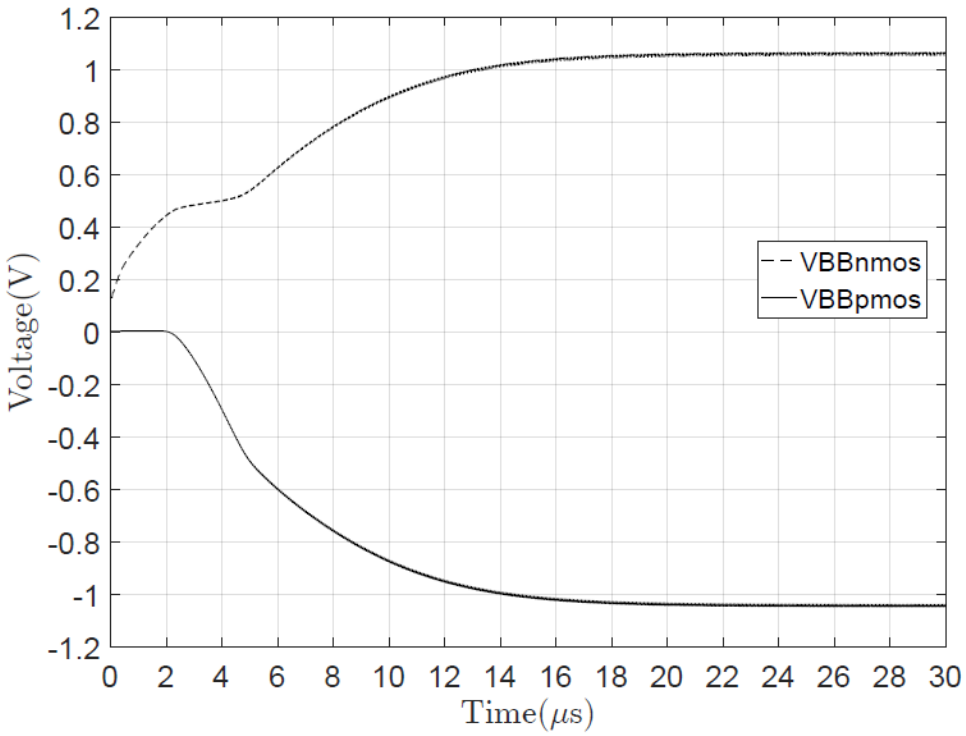

Figure 36. Output voltages of Optimized BBG with FBB feedback in NOC

5.5.3.Optimized BBG with FBB feedback in NOC and GCCCP

The simulation of clocks in the output of NOC is shown in Figure 35 and the output voltages in Figure 36. With the feedback in the NOC, the clock signal is very similar to the ideal one.

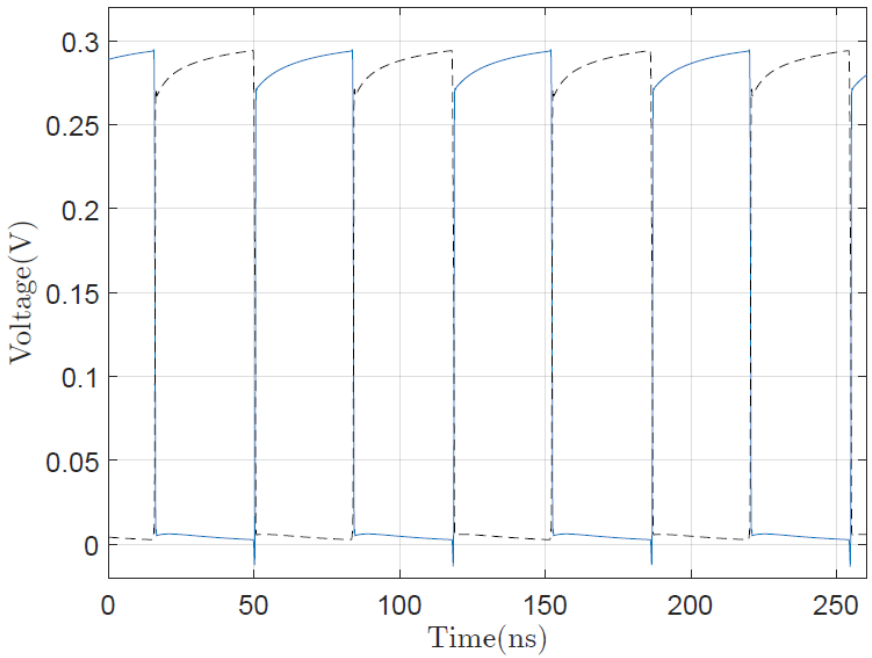

Figure 37. Clock signal with two phases of Optimized BBG with FBB feedback in NOC and GCCCP

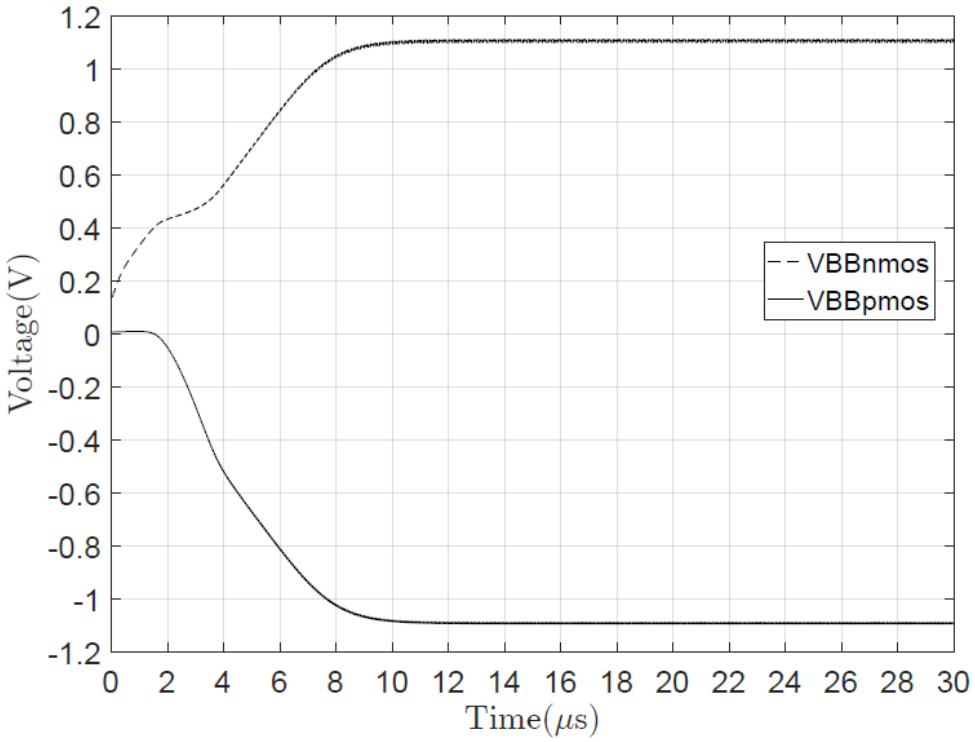

Figure 38. Output voltages of Optimized BBG with FBB feedback in NOC and GCCCP

5.5.4. Analysis of simulation and results

The simulations of this Section reassert the behavior of the BBG explained in Section 5.4. To compare the optimization of the circuit, the same metrics are analyzed for this circuit.

In Table II is shown the values of the metrics for the optimized BBG. If the metrics are compared with the simulation before the optimization, the SSV is only worst in the case of the BB for PMOS when FBB is applied to the circuit. In the case without FBB the values are higher for both voltages.

Table II. Metrics of Optimized Body Bias Generator

Metric	Without FBB	FBB in NOC	FBB in NOC and GCCP
SSV (BB NMOS)	0.884 V	1.066 V	1.111 V
SSV (BB PMOS)	-0.865 V	-1.049 V	-1.096 V
Setting Time (BB NMOS)	16.46 µs	11.6 µs	7.36 µs
Setting Time (BB PMOS)	16.56 µs	11.7 µs	7.47 µs
Power Consumption	350.787 nW	419.882 nW	624.975 nW

In the setting time is analyzed, the time needed for all the cases increases a lot. The reason for this slow charge is due to the frequency of the clock is lower and the power consumption too. The relationship between power consumption and setting time works in the same way

that the BGG without optimization, it means, to reduce the setting time, the power consumption has to be higher due to higher transfer of charges.

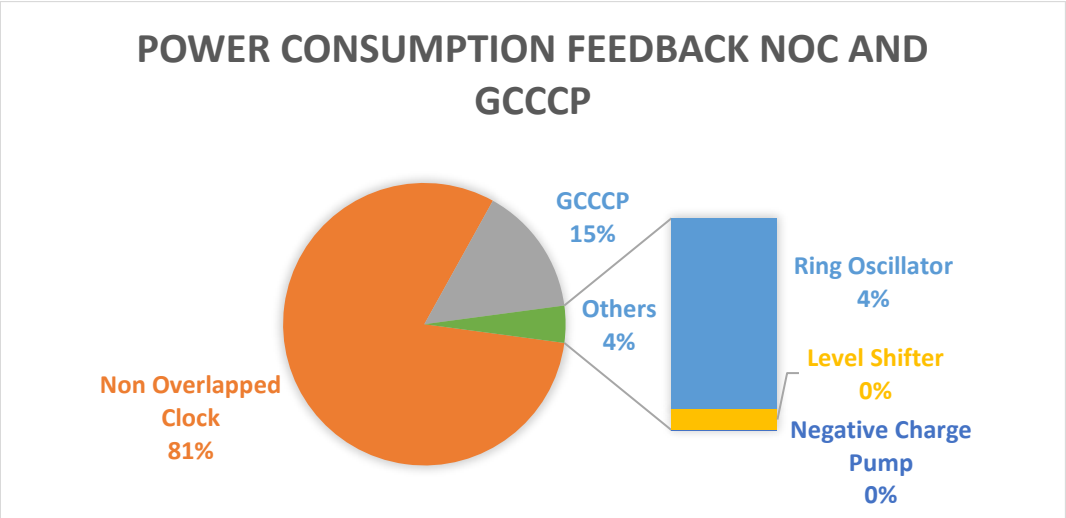

Figure 39. Power consumption of block of Optimized BBG with FBB feedback in NOC and GCCCP

In Figure 39 is represented the power consumption of all blocks of the optimized BBG with FBB feedback in NOC and GCCCP. The most part of the consumption is in the NOC and the GCCCP, because these blocks generates the output voltage from the power supply, clock signal with dual-phase and the V_{IN} of the CP, transferring all the charges needed.

The third block in power consumption is the RO, that it creates the clock signal from the voltage supply. The NCP has a power consumption very low from V_{DD} because the great part of components use the BB of NMOS as voltage supply to generate the BB of PMOS.

In conclusion of the analysis of optimized BBG, it achieve the objectives of the thesis. It generates positive and negative voltages higher than ± 1 V with a power consumption of 1μW. The generation is also faster, around 10 μs to achieve the desired voltage from the beginning.

6

DESIGN OF CIRCUIT OF CONTROL

6.1. Introduction

The application of the Body Bias Generator designed in this thesis is to improve the performance of the ultra-low power electronics circuits. The main objective of this devices is to reduce the power consumption of circuits, then the Forward Body Bias only should be applied when the application circuit requires higher performance, to avoid leakage currents. If the FBB is not required, the BBG is not necessary and the circuit shall be stopped to avoid needless power consumption.

Some circuits and applications do not always require the best performance, it means that the FBB applied should be less that the maximum value. If it possible, the same BBG could be used for different applications, allowing a better control of the gate delay of integrated circuits.

If the BBG could be controlled by a circuit that switch it on when FBB is required and to provide an exact voltage demanded by the application, it is possible to design an efficient voltage generator that could be used in ultra-low power electronics design.

This Chapter details the design of a digital Control Circuit based in the effect on the gate delay of transistors when FBB is applied, effect studied in Section 6.2. Once the effect of FFB is explained, the architecture and design of a first model of Control Circuit is presented in Section 6.3 and in Section 6.4 a second model of Control Circuit is explained.

6.2. Study of Forward Body Bias Effects over Ring Oscillators

As is explained before, when a Forward Body Bias is applied to a circuit, its performance is improved because the gate delay is reduced. The upgrade of gate delay is reflected in the speed of circuits. One of the best circuits to study this effect is the Ring Oscillator, due to the improvement of the gate delay is reflected in frequency of the clock delay.

In the study two Ring Oscillators are used, one of 10.7 MHz and 20.32 MHz, to analyze how affect two circuits with different numbers of logic gates and sizes of the transistors. For both clocks, three cases are studied:

- FBB only in NMOS transistors
- FBB only in PMOS transistors
- FBB in PMOS and NMOS transistors

The first case to analyze is the Ring Oscillator of 10.7 MHz, which is simulated in the three cases. The first case to study is the effect on the frequency when the FBB in applied only in

the NMOS. The results of the simulation are shown in Figure 40. As it is shown, the frequency increase proportionally to the FBB

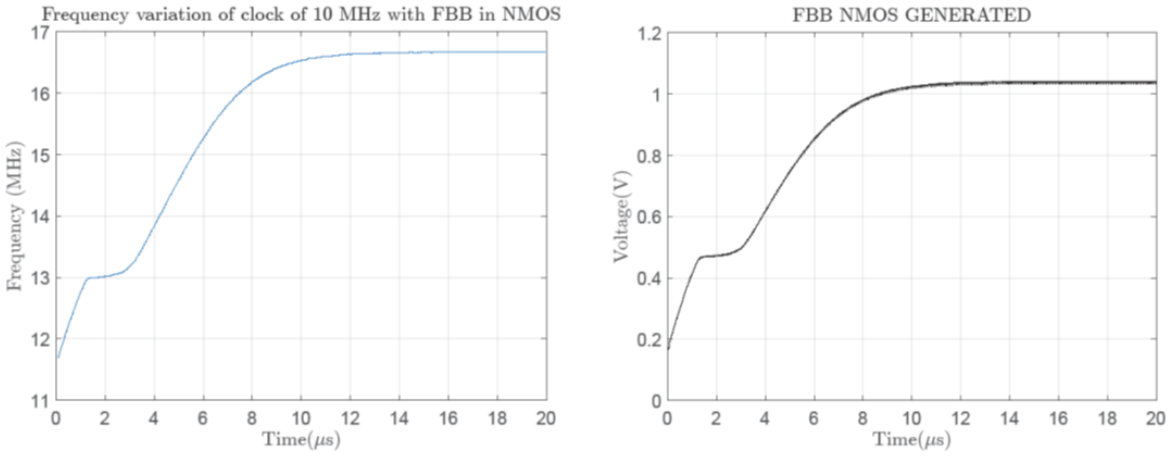

Figure 40. Effect of FBB in NMOS of RO of 10.7 MHz

Figure 41 shows how many times increase the frequency of clock signal respect to the nominal frequency of the RO without FBB. In the case of the positive voltage, the first 200 mV are generated instantaneously, then modification of frequency starts directly at that voltage.

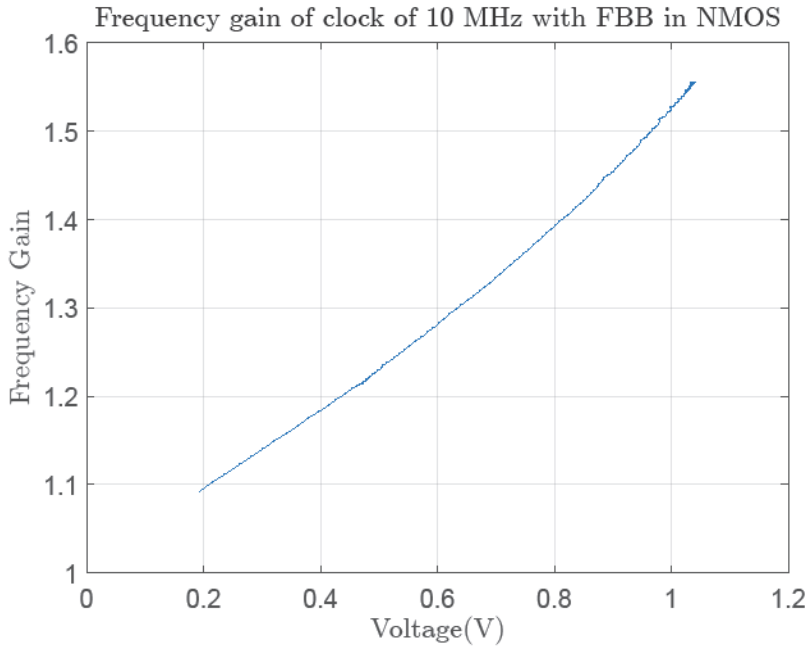

Figure 41. Frequency Gain of RO of 10.7 MHz with FBB in NMOS transistors

The next case to study is when the FBB is applied to PMOS. In Figure 42, the variation of the frequency of RO in relation with the FBB is shown. As it happens in the previous case, the frequency increases proportionally to the FBB.

In Figure 43 the frequency gain due to FBB in PMOS in relation to the nominal value of RO is shown. In this case, the frequency increases higher than the previous case.

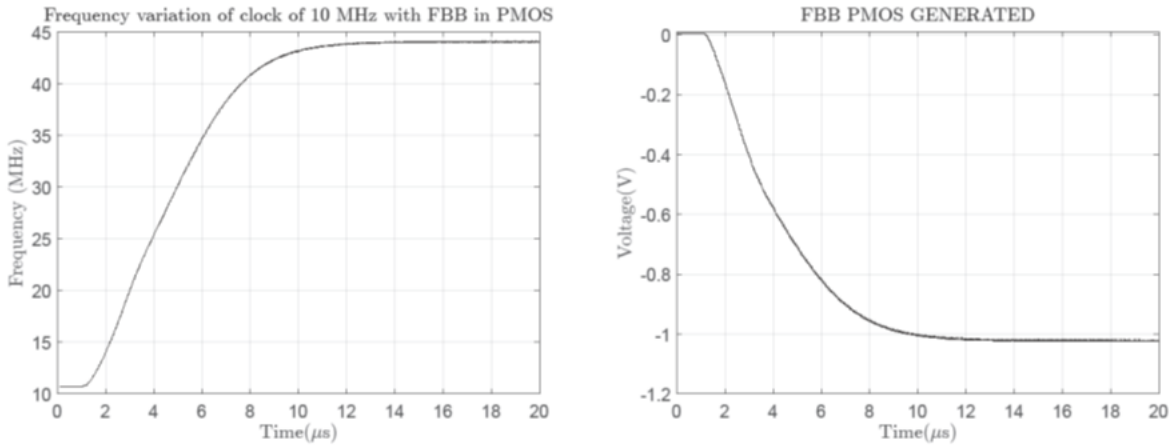

Figure 42. Effect of FBB in PMOS of RO of 10.7 MHz

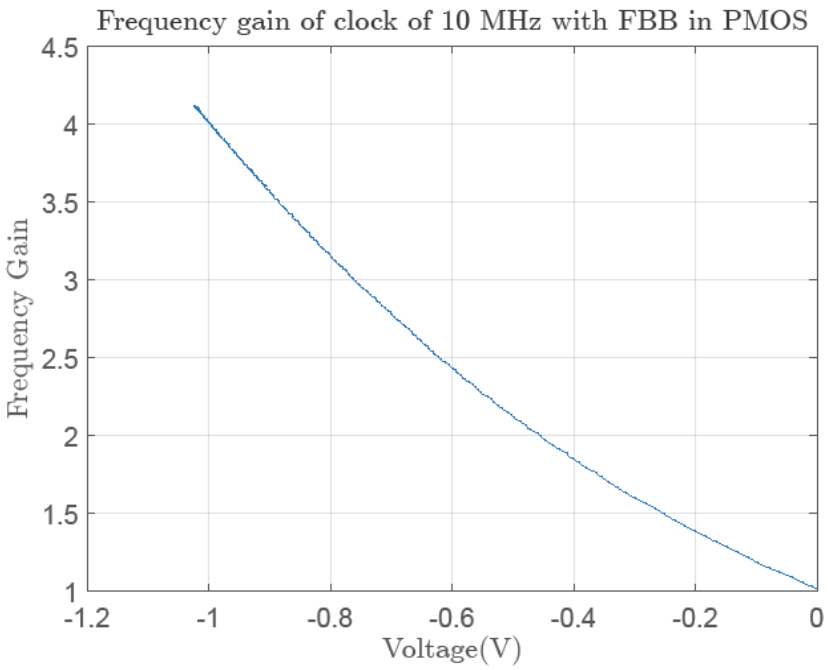

Figure 43. Frequency Gain of RO of 10.7 MHz with FBB in PMOS transistors

In the last case of study, FBB is applied to both transistors, PMOS and NMOS. In Figure 44 is shown how the frequency varies with the FBB, where the predominant effect is due to FBB in the PMOS. It is due to higher gain of frequency due to FBB in PMOS in relation with the FBB in NMOS.

In the case of the RO of 20.32 MHz, the effect of FBB works in the same way, increasing the frequency proportionally to FBB. In Table III are shown the results of frequency's gain in both cases. The results are very similar, providing a good idea of how the FBB affects the behavior of RO made with UTBB FDSOI 28nm.

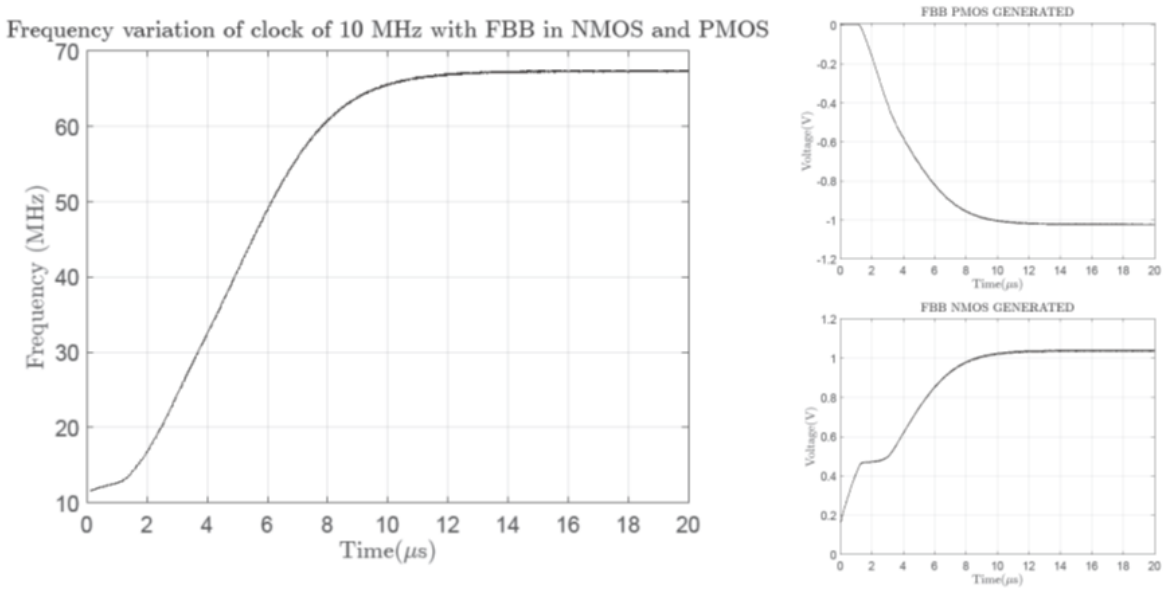

Figure 44. Effect of FBB in PMOS and NMOS of RO of 10.7 MHz

When FBB is applied to the NMOS and PMOS transistors, the effects of the variations due to both FBB are independents, increasing the frequency as

$$Freq_{clk} \approx Freq_{clk_{original}} * Gain_{FBBNMOS} * Gain_{FBBPMOS}$$

With the knowledge of the relationship between the gate delays of the RO with the FBB, the design of the Control Circuit could be based in this results. In the next Sections, a digital Control Circuit using the Ring Oscillator as a voltage-to-frequency converter.

Table III. Gain of Frequency of RO with FBB

Gain of Frequency	FBB in NMOS	FBB in PMOS	FBB in PMOS and NMOS
RO of 10.7 MHz	1.52	4	6.3
RO of 20.32 MHz	1.5	3.9	6.3

6.3. Design of First Control Circuit

In this first model Control Circuit, the idea is to use the behavior of the Ring Oscillator to increase the frequency of the clock generated applying the Forward Body Bias to their transistors. In Figure 45 is shown the architecture of this first Control Circuit.

To control the voltage generated by the Body Bias Generator, the circuit use two Ring Oscillators:

- One with a fixed frequency, which works as a Reference's Clock.
- Another with a variable frequency controlled by the FBB applied, that works as Control's Clock.

This two clock signal are used to create a counter of N bits, which counts how many rising edges has the Control's Clock when the Reference's Clock is in high level. The Reference's Clock has to be

$$f_{ref} = \frac{f_{control}}{(2^N - 2) * 2}$$

, where $f_{control}$ is the frequency of the maximum voltage desired, it means, the frequency of the RO when ±1 V is applied as FBB.

The result of the counter is divided by two, truncate 1 bit, to avoid the problems of have an incomplete cycle of the Control's Clock inside the high level of the Reference's Clock. It provides more stability to the circuit.

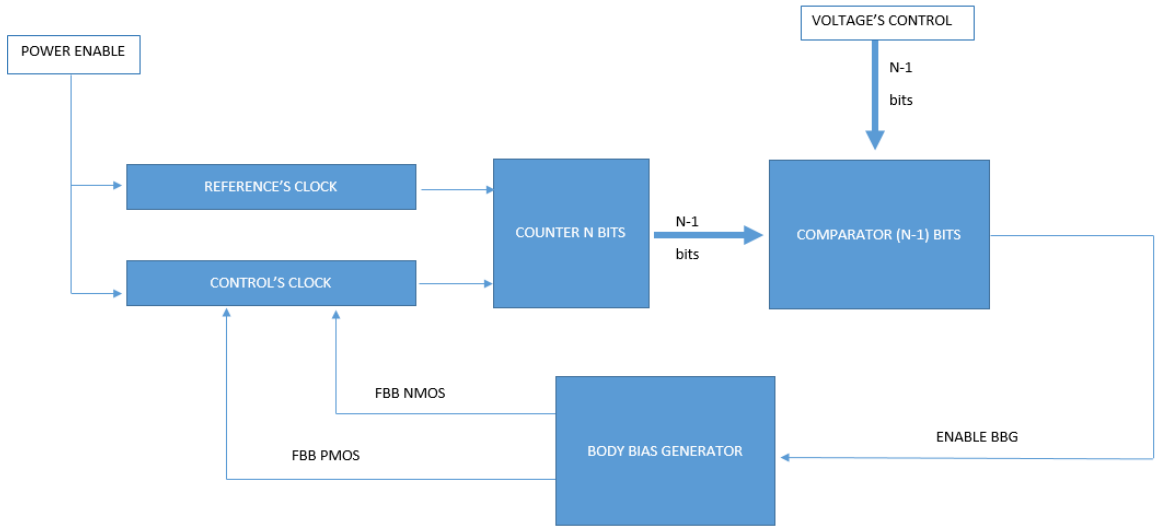

Figure 45. Architecture of the first model of Control Circuit

The truncated value is compared with the input Voltage's control, N-1 bits, and if the value is lower, the output signal, Enable BBG, enables the FBB generation until the truncated counter reach the same value of the input. The input Power Enable can activate or deactivate the Body Bias Generation and the Control Circuit. To improve the performance of the Control Circuit, FBB is applied in Counter and Comparator blocks.

To design the blocks of this First Control Circuit, the clock are RO oscillators that are designed as it is explained in Section 5.3.1. For the counter and the comparator, the design of the circuit was different, using a design in Hardware Description Language, HDL.

The first step for the design HDL is to create a code in one of the two HDL options, VHDL or Verilog. In this case, VHDL is used to model the Control Circuit. One the code of the model is created and tested, the next stage is to pass the VHDL, a high-level programming language, to a Verilog, a low-level programming language.

The transformation of HDL is needed, because the Cadence tools needs a Verilog model to design the circuit automatically with the library specified for the design. To translate the VHDL to Verilog model, the Synthesizer of Cadence is used. In this Software Tools is needed to select the libraries for the design, the model of the circuit and the constraints. The

result is a Verilog model with the required cells of the library and the interconnection of the nets. With the final Verilog model and the constraints, it is also possible to obtain different reports to estimate the power and area required by the circuit. Table IV shows the estimation done by the Synthesizer of Cadence for the First Control Circuit with N=3, where the results serve to have an idea to compare designs. The power estimation is more dependent of the voltage supply and frequency of the circuit.

Table IV. Estimation of power consumption and area for First Control Circuit with N=3

Power Consumption		
Leakage	**Dynamic**	**Total**
160.239 nW	2.737 µW	2.897 µW
Area Estimation		
Cells	**Nets**	**Total**
25.949 μm^2	29.178 μm^2	55.127 μm^2

Finally, the Verilog model obtained in the Synthesizer of Cadence could be used in the Cadence Virtuoso, where all the design are done for the complete circuit of this thesis. With the design implemented, it is possible to simulate the circuit.

In this case, the circuit, the simulation, as the implementation, is done for N=3 bits and the Control's Clock is a RO of 20.32 MHz. As N=3, the theoretical number of voltages to be controlled are four, being the maximum voltage controlled ±1 V. The simulation are done for three cases of FBB on the RO,

- FBB only in NMOS transistors.
- FBB only in PMOS transistors.
- FBB in PMOS and NMOS transistors.

, and the design and results are explained in the following Subsections.

6.3.1. First Control Circuit with control FBB in NMOS

In the case of the FBB in NMOS, the frequency of the RO oscillator of 20.32 MHz increases up to 30.49 MHz when the voltage is 1 V. The first step to design this First Control Circuit is to set the Reference's Clock up. The frequency reference, f_{ref}, is calculated as

$$f_{ref} = \frac{f_{control}}{(2^N - 2) * 2}$$

, where the result is 2.54 MHz.

Once that both RO are designed, the simulation can be done. In Figure 46 the result of the simulation is shown, where the variation of frequency of Control's Clock is drawn in blue, the frequency that can be controlled is sketched in different colors and drawn in black dotted lanes are the frequencies correspondent to the truncated values of the counter. In this case, as the variation of the frequency is not high enough, the First Control Circuit works as an

on-off controller, wasting two values of control. This circuit provides in the output of the BBG a stable 1 V.

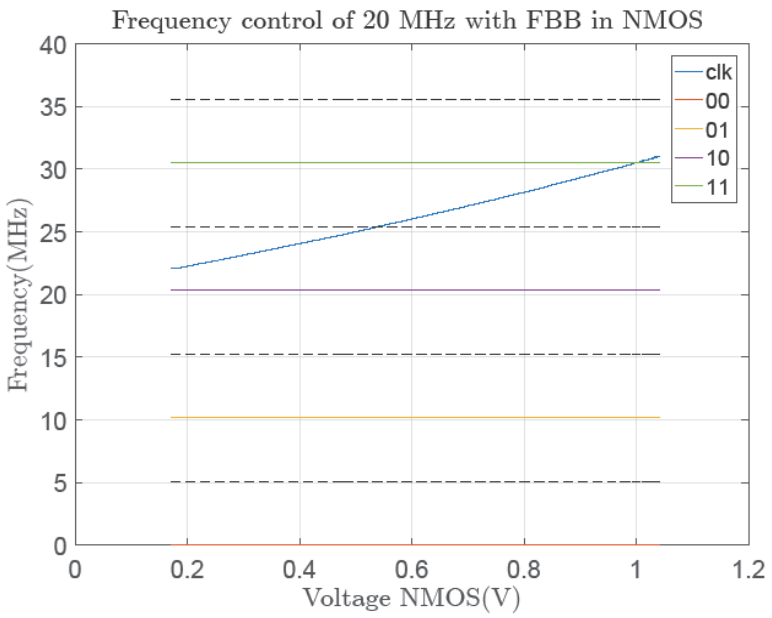

Figure 46. Simulation of the First Control Circuit based on RO with FBB in NMOS

6.3.2.First Control Circuit with control FBB in PMOS

In the case of the FBB in PMOS, the frequency of the RO oscillator of 20.32 MHz increases up to 79.95 MHz when the voltage is -1 V. For this case, the f_{ref} is 6.66 MHz.

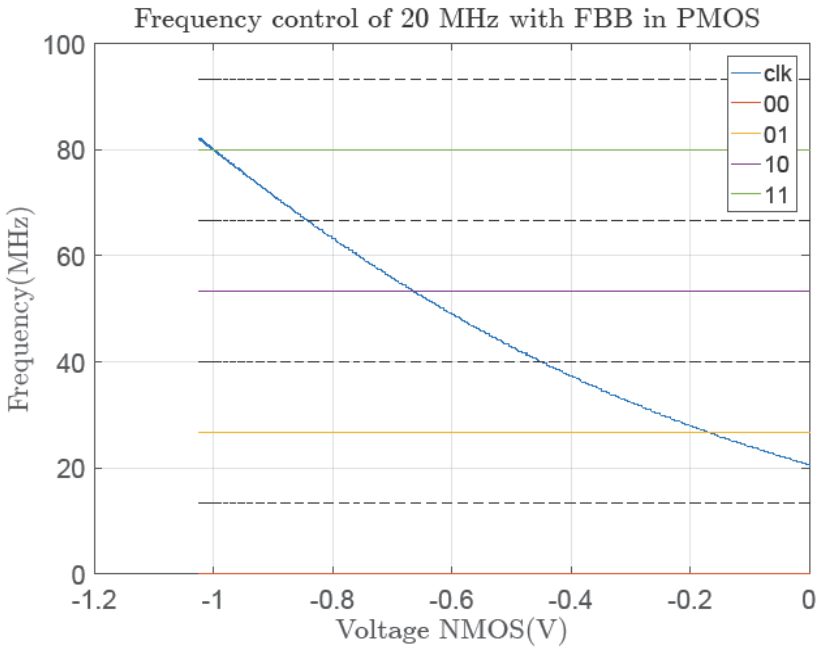

Figure 47. Simulation of the First Control Circuit based on RO with FBB in PMOS

Figure 47 shows the simulation of the circuit, with the same characteristics in the representation as the last case. In the simulation of this case, as the variation of frequency is higher, the voltage that can be controlled are four, using all the possible values.

6.3.3.First Control Circuit with control FBB in PMOS and NMOS

In the case of the FBB in PMOS, the frequency of the RO oscillator of 20.32 MHz increases up to 121.25 MHz when the FBB is 1 V in NMOS and -1 V in PMOS. For this case, the f_{ref} is 10.10 MHz.

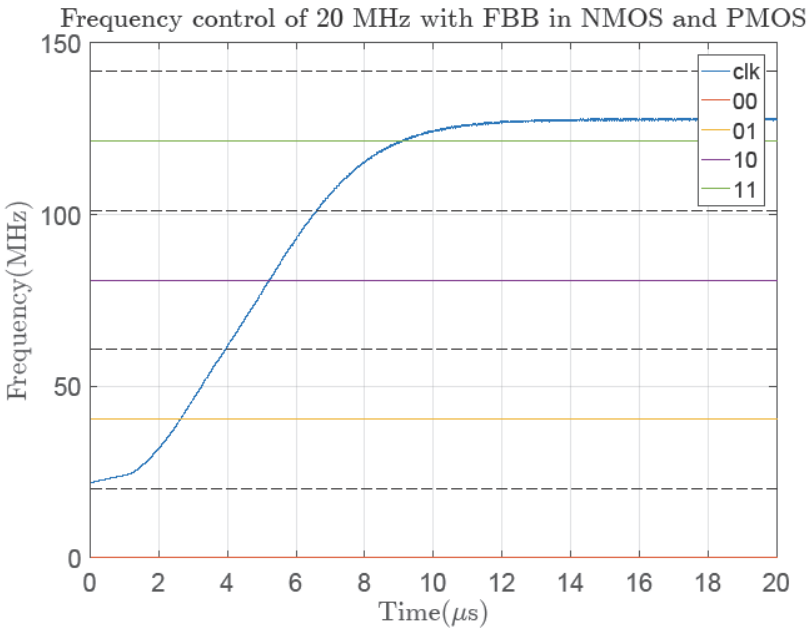

Figure 48. Simulation of the First Control Circuit based on RO with FBB in PMOS and NMOS

In Figure 48, is represented the values of control in relation with the frequency of the RO. In this case, as the frequency depends on the FBB in PMOS and NMOS and the BBG cannot generates symmetrical voltages, especially in low voltages, due to its behavior and losses. In Table V are the correspondence between the control bits and the values of voltage controlled.

Table V. Output voltages for the First Control Circuit with control of FBB in PMOS and NMOS

Binary Value	FBB in NMOS	FBB in PMOS
00	0 V	0 V
01	0.482 V	-0.316 V
10	0.773 V	-0.736 V
10	1.010 V	-0.989 V

6.3.4. Analysis and Conclusion of First Control Circuit

Once of all the cases are simulated, it is possible to realize that with this circuit, it is possible to control the voltage generated by the BBG, working better as the gain of the frequency in the RO is higher. But this circuit has many drawbacks,

- The design of two clocks with different frequencies. As the difference of frequency is so high when the FBB is applied, the difference of both frequency, makes that the Reference's Clock has to be slow, few MHz. It makes that the control of the voltage generated is also slow.
- In the case of FBB in PMOS and in PMOS and NMOS, it is possible to control intermediate values. The problem of intermediate voltage is its instability, being worse when the voltage is lower. It is due to the generation in the first steps of BBG is very fast, making the variation higher and providing a worst voltage in the output. This effect is more significant if the control is slow, as in this case, generating an output voltage with a very high variation.
- The scalability of this circuit is not easy due to problems with frequency. When the number of bits increases, the difference between the Control's frequency with ±1 V of FBB and the Reference's frequency is much higher.

  It means that the two possibilities are not viable, because if the Control's Clock is the same, increasing the number of bits N, its Reference's Clock shall be slower, getting worse the control with more variability in the output voltage. The other option is to use the same Reference's Clock, that it cause a study of a new RO for the Control's Clock and maybe being impossible that the circuit works, due to the limitation of higher working frequencies.

For these drawbacks, a new model for the Control Circuit is designed and it is explained in the next Section.

6.4. Design of Second Control Circuit

Due to the complexity and inefficiency of the First Control Circuit, a new design is proposed. The Second Control Circuit is based in the same theory of the effect of the FBB applied to RO and it is very similar to first one.

In Figure 49 is shown the architecture of the Second Control Circuit. The architecture is basically the same as the first model explained in Section 6.3, but the operation of each block changes.

In the Second Control Circuit, the Reference's Clock and the Control's Clock uses identical RO. It eases the design of the control circuit, because it is not necessary the study of the performance of RO and avoid the calculation and design a second RO. Another advantage is as the difference between the nominal frequency of the RO, used as Reference's Clock, and the frequency when FBB is applied, being in the worst case a difference of 6 times approximately.

The big difference between both models is the Counter block. In this case the counter increases to indicate the frequency's gain of the Control's Clock, in relation with the original

frequency, Reference's Clock. As the difference of frequencies is lower, the control works faster and the results of the counter doesn't need to be truncated.

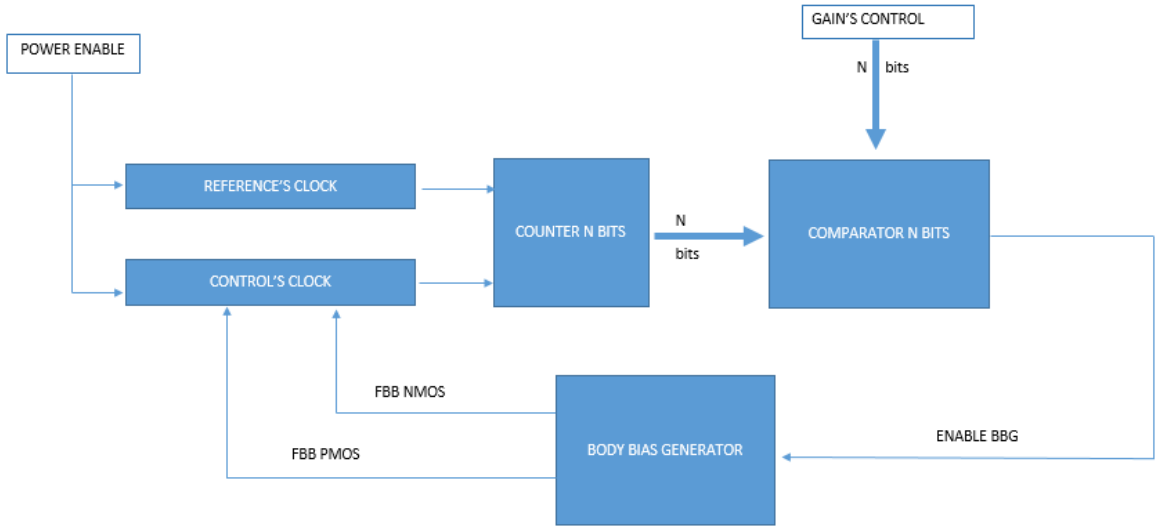

Figure 49. Architecture of the Second Control Circuit

The output of the Counter is compared with the control of gain required by the user. The best case is to use FBB in PMOS and NMOS because, as it is shown in Table III, the gain is approximately 6.3 times for the RO designed in technology of 28 nm UTBB FDSOI. It is the best option, because the possibility of gain is higher. In this Section, the design of the Second Control Circuit is explained for the case with FBB in PMOS and NMOS. As is done in the first model, FBB is also applied to Counter and Comparator blocks to improve its performance.

To design the model of the Control Circuit, the first parameter to select is the number of bits used to control the output voltage. Using FBB in NMOS and PMOS, the gain frequency is 6.3 as is showed in Table III. To achieve the control of the maximum gain, at least N=3 bits are required.

Another great advantage of this model, is the scalability. To achieve a better control of the voltage generated, the number of possible values are duplicated only by adding 1 bit to the Counter and Comparator and a frequency divider between the Reference's Clock and the Counter. The Second Control model eases the scalability, because if we want to increase M bits to the basic circuit, it is only needed that the frequency divider provides an output clock signal, whose frequency is modified by a factor of $\frac{1}{2^M}$.

To design the Second Control Circuit, it used the same process as was explained in Section 6.3. For this circuit, two VHDL models are used, one for the control circuit with 3 bits and other with 4 bits. Besides the number of bits, two strategies are used for the design, one for each VHDL model.

The circuit with 3 bits, is the basic model for the Control Circuit with FBB in PMOS and NMOS. The strategy used in the design is to create a VHDL model where the Counter and Comparator are designed together. The estimation of power consumption and area are in Table VI.

Table VI. Estimation of power consumption and area for Second Control Circuit with N=3

Power Consumption		
Leakage	**Dynamic**	**Total**
302.442 nW	642.686 nW	945.128 nW
Area Estimation		
Cells	**Nets**	**Total**
45.043 μm^2	29.339 μm^2	74.382 μm^2

To control a great number of output voltages, it is possible to increase the number of bits. In this case, an extra bit is added to the basic model, having 4 bits of control. The strategy used in the design is to create a VHDL model for each block, one for the Frequency Divider, other for the Counter and another for the Comparator. The results of estimation for each block are shown in Table VII. The difference in respect of the estimation of the previous model is that the Synthesizer of Cadence in this case optimize each block independently and not as a unique circuit.

This strategy of design doesn't optimize the complete circuit, then the connection of blocks and the estimation of power and area could be worse, but it eases the replacement of specific blocks, therefore the prototypes of different models could be switched faster. Once the model is tested, the recommendable is to optimize the circuit by the design of the entire circuit as unique block, with some possible improvements in area and power consumption.

Table VII. Estimation of power consumption and area for Second Control Circuit with N=4

Blocks	**Power Consumption**			**Area Estimation**		
	Leakage	**Dynamic**	**Total**	**Cells**	**Nets**	**Total**
Freq. divider	30.78 nW	196.29 nW	227.07 nW	5.22 μm^2	3.11 μm^2	8.33 μm^2
Counter	212.42 nW	1.50 µW	1.71 µW	37.86 μm^2	44.67 μm^2	82.53 μm^2
Comparator	20.23 nW	608.59 µW	628.82 nW	18.67 μm^2	9.30 μm^2	27.97 μm^2
Total	263.43 nW	2.305 µW	2.568 µW	61.75 μm^2	57.08 μm^2	118.83 μm^2

If both model of the Second Control Circuit are compared, the power consumption and area increases with the number of bits used. It is as expected, because a bigger number of bits implies more cells to be used.

The model of 4 bits is the control circuit selected to do the simulation of overall circuit, BBG and Control Circuit, to be analyzed more in detail in the Chapter 7.

7

SIMULATION OF BODY BIAS GENERATOR AND CONTROL CIRCUIT

7.1. Introduction

In this Chapter, the simulation of the complete circuit, the Body Bias Generator and the Second Control Circuit, is done and analyzed in detail. The structure of the complete circuit is shown in Figure 49, using N equal to 4.

The FBB is applied to PMOS and NMOS transistors of the Control's clock. The selected RO has a frequency of 20.32 MHz. For the simulation, the values chosen for pumping capacitors, C_{CH} and C_{fly}, are 200fF and for the load capacitor, C_L, is chosen 1 pF. The value of the C_L is high to simulate the parasitic capacitance of the transistors of a complex circuit, with a great number of transistors. The simulation is done for all combination of the 4 control bits.

In the results, voltage generated by the BBG, frequency variation and the power consumption are analyzed in detail.

7.2. Results

The first parameter to analyze is the frequency's variation of the RO for all the cases. In Figure 50 is shown how the frequency of the Control's clock is incremented when the value of the control bits are higher. In the first three values of control, the frequency is the same to the original, because the frequency cannot be lower than the original by applying the FBB. For higher frequencies, the last two control values has the same frequency. It happens because the FBB cannot be increased more, therefore the frequency reaches his maximum.

Another thing to realize, is that the frequency of the Control's Clock is not exactly a multiple of the original frequency as is expressed in the equation

$$freq_{control} = \frac{1}{2} \cdot Control_{value} \cdot freq_{reference}$$

It happens because the frequency of the Reference's Clock after the frequency divider is modified a few kHz, being lower the reference' frequency for high FBB. The reason is that faster is the counter, the demanding of current is higher, modifying the speed of transitions, therefore the quality of the signal is deteriorated. In Figure 51 is shown the relationship between control and reference frequencies in the input of the counter, where the values obtained are the expected in relation with the design and the behavior of the RO, being the gain 6.3 times the original when the FBB is applied. The gain is represented in function of the half of the original frequency of RO.

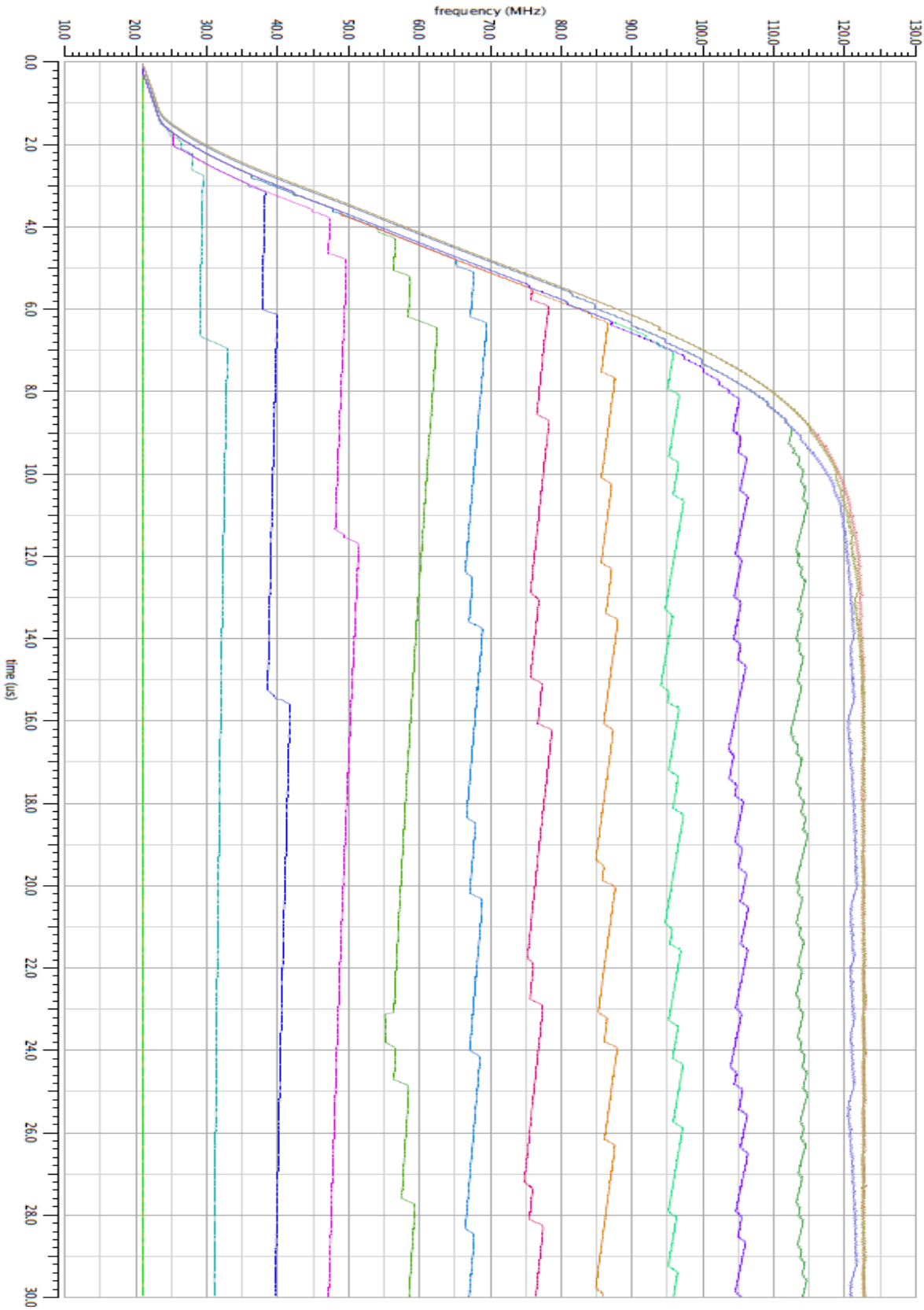

Figure 50. Frequency of Control's Clock in all cases of control

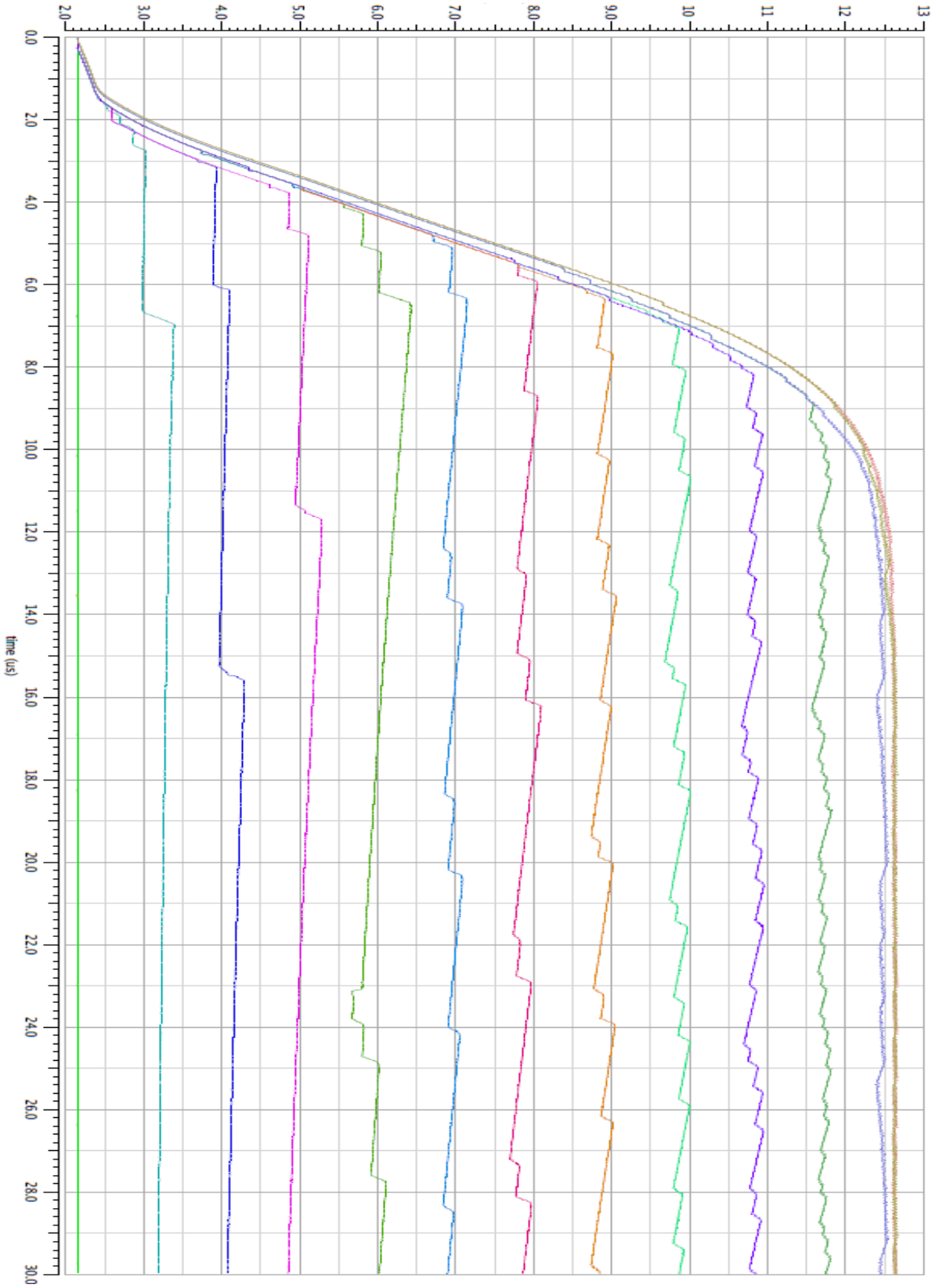

Figure 51. Gain of Control's Clock in relation of Reference's clock after the frequency divider

Table VIII shows the resume of the relationship between the frequency of Control's Clock and the control bits. As it was explained before, the difference between the ideal frequency's gain and the real is due to the modification of the input reference's clock of the Counter. This difference is also multiplied by the gain, being more important for the higher values of control.

If the input gain of the Counter is observed, the values are the very similar to the ideal. In this case, to obtain the real gain of the Control's Clock, this gain has to be divided by two, due to use the half of the frequency of Reference's Clock in the Counter.

Table VIII. Resume of frequencies of Control's Clock after control

Control Binary Value	Control's Clock Frequency(MHz)	Real Frequency's Gain	Input Frequency's Gain of Counter
0000	20.32	1	2.00
0001	20.32	1	2.00
0010	20.32	1	2.00
0011	31.02	1.53	3.03
0100	39.89	1.96	4.04
0101	49.65	2.44	5.02
0110	59.30	2.92	5.98
0111	68.84	3.39	6.95
1000	76.03	3.74	7.92
1001	86.51	4.25	8.90
1010	96.63	4.76	9.89
1011	104.73	5.16	10.86
1100	114.26	5.62	11.79
1101	121.35	5.97	12.48
1110	122.85	6.05	12.65
1111	122.85	6.05	12.65

The next parameter to analyze is the voltage generated by the BBG for each value of the control. In Figure 52 is shown the generation of NMOS' BB and in Figure 53 the BB of PMOS. Table IX shows the resume of all steady state voltage for each case.

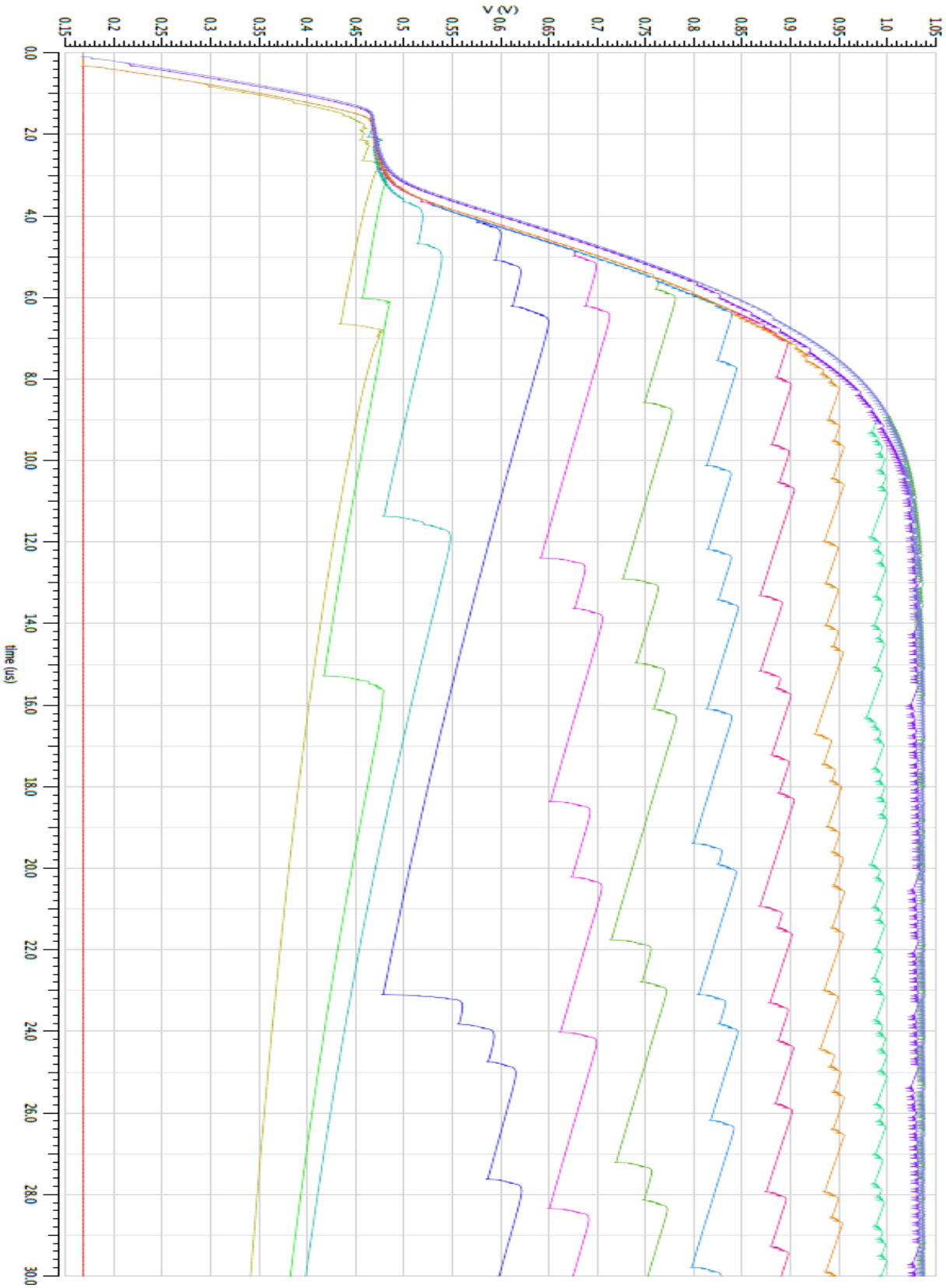

Figure 52. Positive voltage generated by the BBG for all cases of control

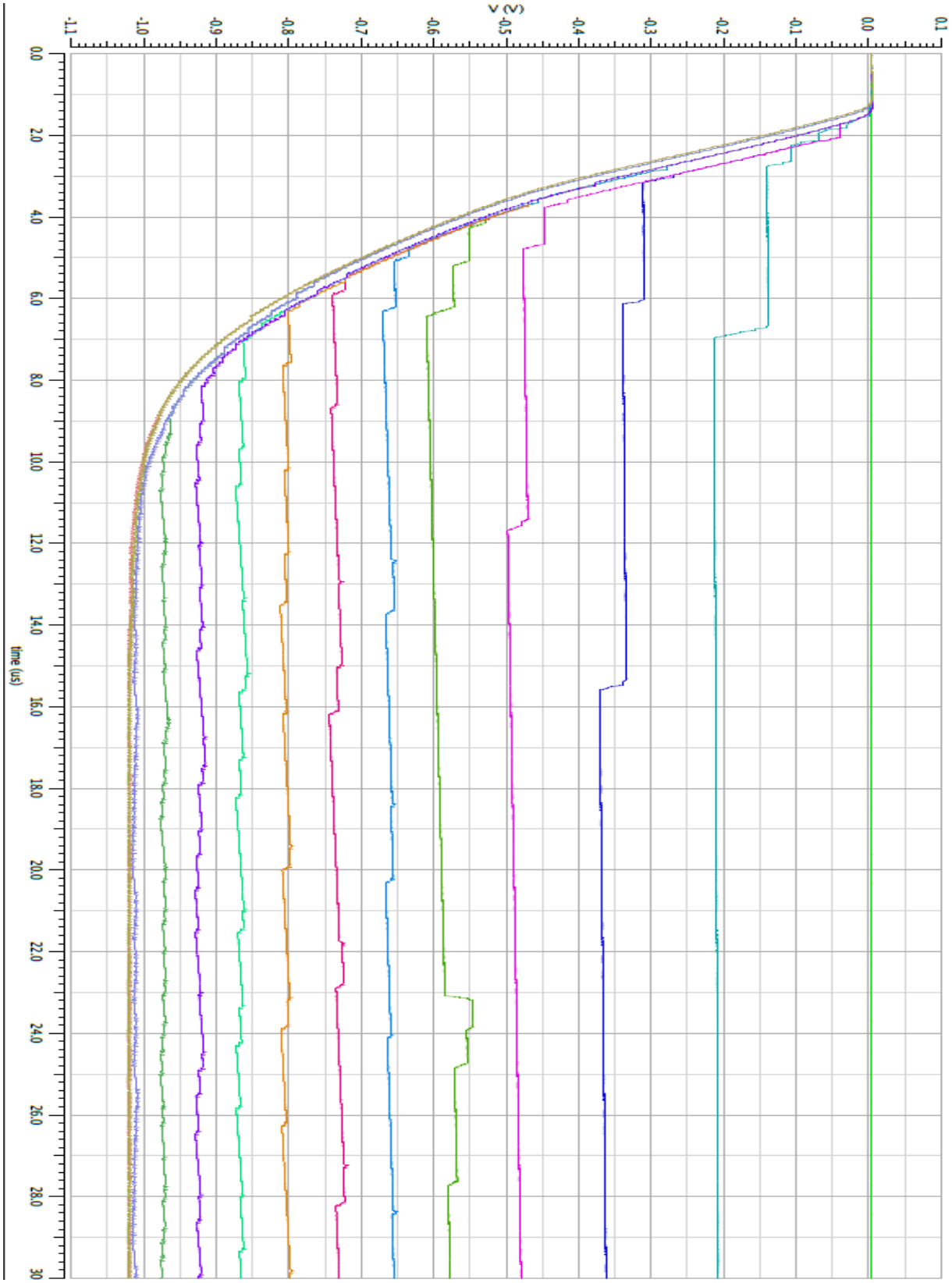

Figure 53. Negative voltage generated by the BBG for all cases of control

If the simulations are analyzed, it possible to observe the difficulty of control the generation of low FBB voltage. It is caused by the behavior of the BBG, where the generation of voltages works as a charge of capacitor, being so fast in the first steps and lower near the steady state voltage, therefore the stability of the control for these values is not easy to achieve due to sensitivity to variation. For high voltages, the variation is smaller because the charge and discharge are slower.

Another thing to observe is the instability of positive voltage is higher than in negative voltage. The reason is that the demand of current of the positive voltage is higher, because its load is the CL and the Negative Charge Pump. It causes the faster discharge of load capacitor, so the higher variation of voltage. The other reason for the instability, is that the RO is less sensitive to variations of FBB in NMOS transistors, requiring more time to detect the variation of voltage.

Table IX. Resume of voltage generated by the Body Bias Generator

Control Binary Value	FBB of NMOS (V)	FBB of PMOS (V)
0000	0.169	0
0001	0.169	0
0010	0.169	0
0011	0.454	-0.212
0100	0.486	-0.359
0101	0.540	-0.488
0110	0.616	-0.580
0111	0.705	-0.666
1000	0.756	-0.735
1001	0.833	-0.809
1010	0.898	-0.873
1011	0.950	-0.923
1100	0.992	-0.976
1101	1.033	-1.011
1110	1.038	-1.022
1111	1.038	-1.022

Finally, the last parameter to analyze in this simulation is the power consumption of overall circuit. In Table X is shown a resume with the power consumption of all the blocks and the total power consumption of the circuit.

As it is expected, the power consumption of the complete circuit increase when the voltage generated is higher.

The power consumption is more evident in the Control Circuit, due to the increase of working frequency. This block is more dependent of the frequency of the Control's Clock, because it works at the same frequency, therefore the dynamic power consumption of all inside cells is higher.

It is also important the power consumption of the BBG, that grows up similar to an exponential way up to the maximum value, as it is shown in Figure 54. If it is avoid the generation of the maximum voltage by the BBG, a great reduction on the power consumption could be achieved. It is an important parameter to optimize the power consumption of the circuit.

For example, in this thesis is desirable to generate ±1V, provided by the circuit when the control value is 1101. It means that is possible to reduce the power consumption in 100 nW respect of the worst case. The reduction is higher if it uses the control value 1100, providing a voltage near to the required with a power reduction of 215 nW on the BBG and 50 nW in the Control Circuit, designing a complete circuit with a power consumption of 1.037 μW. This last scenario is near to the objective of the thesis to design a voltage generator, which provide ±1 V with a consumption of 1 μW or lower.

Table X. Resume of overall power consumption in all cases

Control Binary Value	BBG (nW)	Ref. Clock (nW)	Control Clock (nW)	Control Circuit (nW)	Total (nW)
0000	10,384	19,282	21,493	156,724	207,883
0001	10,384	19,282	21,493	157,926	209,085
0010	10,384	19,282	21,493	157,941	209,100
0011	11,869	19,269	31,811	223,079	286,028
0100	13,186	19,260	39,972	270,849	343,267
0101	14,298	19,257	46,928	305,702	386,185
0110	40,045	19,256	58,887	382,756	500,944
0111	39,790	19,256	67,875	437,774	564,695
1000	59,895	19,256	76,984	503,083	659,218
1001	58,490	19,256	87,727	563,815	729,288
1010	73,112	19,256	98,042	634,138	824,548
1011	96,717	19,256	108,139	701,326	925,438
1100	134,859	19,257	117,254	764,779	1036,149
1101	247,438	19,258	124,940	818,151	1209,787
1110	351,300	19,258	126,589	817,627	1314,774
1111	351,393	19,258	126,547	817,995	1315,193

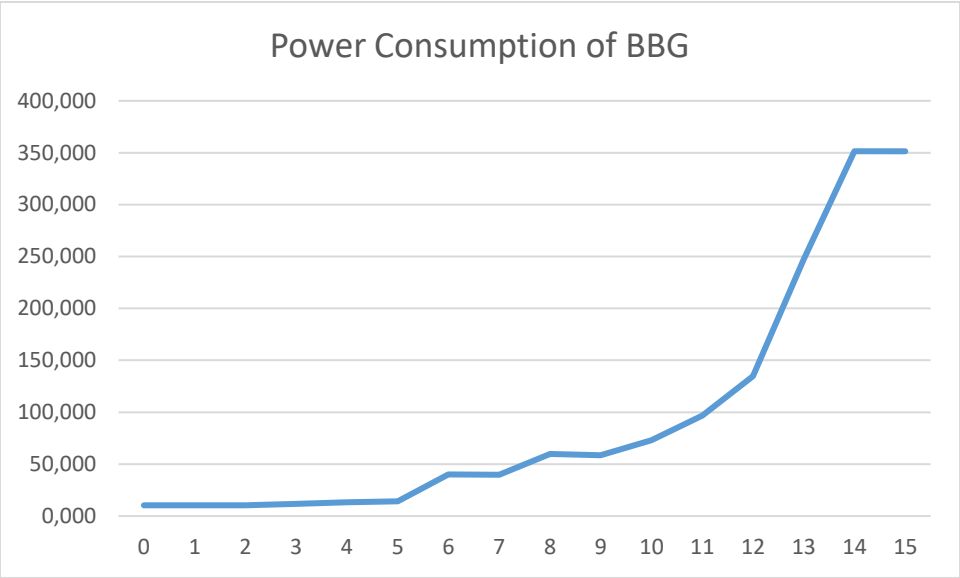

Figure 54. Power consumption of BBG

In Figure 55 are compared the distribution of power consumption for the cases explained before. In is important to realize the exponential consumption of the BBG, increasing in importance its power consumption.

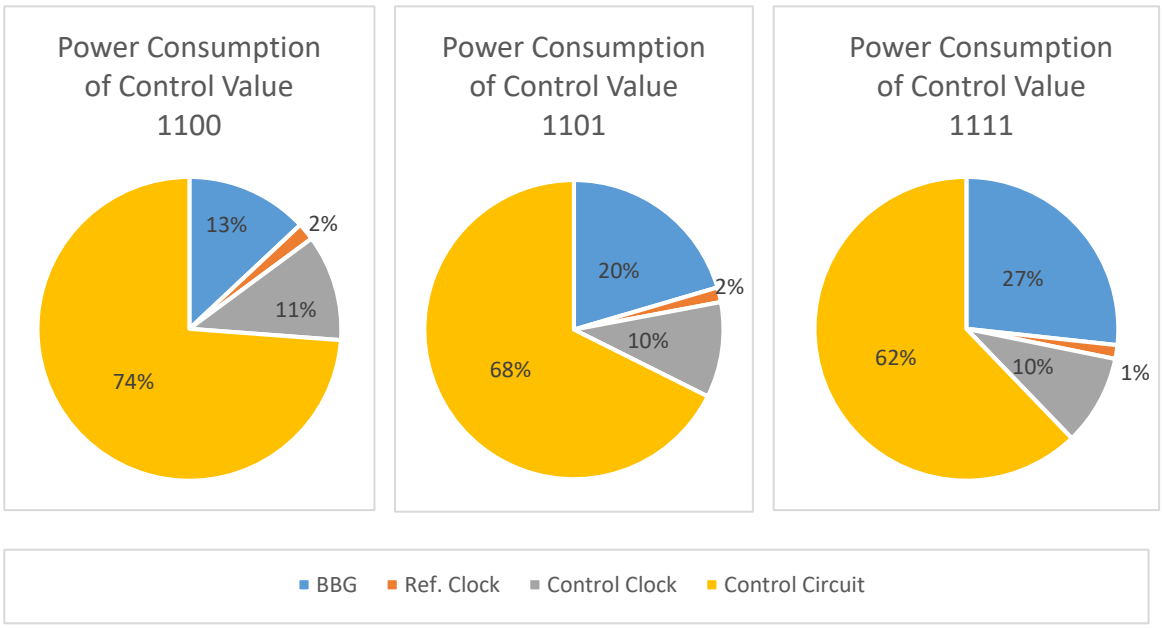

Figure 55. Distribution of the power consumption for higher control values

8

PHYSICAL CAPACITORS: EFFECTS INTO THE BODY BIAS GENERATOR

8.1. Introduction

Once the complete circuit, BBG and Control Circuit, is simulated and verified, the next step in the design process is to replace the ideal components for the real ones. In the model simulated in Chapter 7, the ideal components used are the pumping capacitors, C_{CH} and C_{fly}, and the load capacitor, C_L. In the case of load capacitor, the ideal model could be used, because it only simulate the capacitance of the possible loads where the Body Bias are connected.

To replace the ideal capacitor, the 28 nm UTBB FDSOI technology provides many options to implement capacitors. In this Chapter, the selected capacitor is EGNCAP.

8.2. Replacement of Capacitors

The EGNCAP are capacitors made by MOSFET of 28 nm UTBB FDSOI. To create a capacitor by a MOSFET, drain and source has to be connected. This is a basic option to create capacitors in Integrated Circuits, avoiding the use of specific tools or techniques in fabrication, therefore the cost of the fabrication could be lower.

In the case of the EGNCAP, the modulation of the capacitance is done by the setting of length and width of the gate. If the model of the capacitor, including parasitic effects, is studied, it is noticed the parasitic capacitance of the body, one the principal effects, which degrades it behavior. This capacitance is created between the body, one of the plates, the thin buried oxide, the isolator material, and the transistor [24]. It is important to take into account fringe capacitors created between the gate and drain or source. One of the plates is the gate and the other the connection between source and drain. The isolation material in this case is the oxide below the gate. Figure 56 shows the parasitic effects included in the model of the EGNCAP, where C_{fringe} is the fringe capacitor, the $R_{juntion}$ is the resistance between source and drain and the channel of the transistor, $R_{channel}$ is the resistance of the channel and the C_{body} that is the capacitance due to the buried oxide of the UTBB FDSOI technology.

As the model of the EGNCAP has a limitation of size, some possibilities to increase the value are possible. The first idea is to put some capacitor in parallel to increase the total capacitance. This technique is not so efficient due to the parasitic capacitance, that it is also increased in the same manner. The other option is to increase the number of gates used to build the capacitor. That is the option used in this Section.

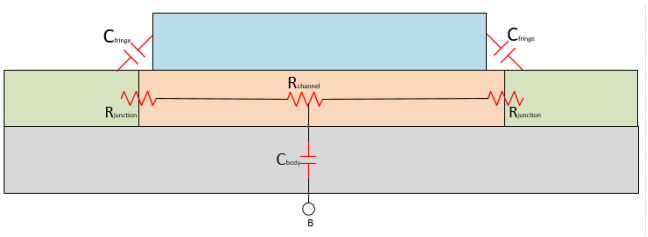

Figure 56. Parasitic effects on the transistors

If we want to replace the ideal capacitors of the BBG, C_{CH} and C_{fly}, by the EGNCAP, the first is to make the calculation of area needed. For the ENGCAP the capacitance is 10.1 fF/μm^2 [14]. Then, to design a capacitor of 200 fF, 20 μm^2 are required. If the same model of BBG of Section 7 is tested with the real capacitors, the voltage obtained is far away of ±1V. For this case less than 400 mV are generated for the positive voltage and 0 V for the negative. Then to achieve the generation of ±1 V, the BBG has to be redesigned the sizes of the components. It is also important to realize, that the EGNCAP may use FBB to modify the value of capacitance.

8.3. Simulation and results

To simulate the circuit, the model of EGNCAP is chosen. In the model of the simulator, the nominal value of capacitance per 1 μm^2 is 2.8649 fF for -1.8 V and 8.86449 fF for 1.8 V. With this new values of capacitance, the area required for the capacitance has to be bigger. Another important parameter to take into account when the EGNCAP are placed, is the polarity of the capacitor, because it could made that the capacitor works correctly or not.

The simulation of the BBG is done with different clock's frequencies and with the optimized BBG of Section 5.5, a BBG with EGNCAP without FBB and a BBG with EGNCAP with FBB feedback . The sizes of capacitors are 4 gates with L=10 μm and W=3.8 μm for C_{CH} and 1 gates with L=10 μm and W= 2 μm for C_{fly}. The clock used to study the different cases is an ideal clock signal provided by a pulse generator.

In the best case, with a frequency clock of 2 MHz, voltage generated is 806.50 mV for BB of NMOS and -536.94 mV for BB of PMOS. These values are far away of the desired one, especially in the case of negative voltage. In Figure 57 is shown the results of the simulation for a clock of 2 MHz for the cases of real capacitors, because when a frequency clock of 14.5 MHz is used, as in the ideal case, the body bias generation is worse. In that Figure are represented in red the ideal case, in blue the case of EGNCAP with FBB feedback and in green the case of EGNCAP without FFB feedback.

It is also important to realize the relationship between the voltage generated and the frequency clock. It could be important to take this parameter into account to optimize the voltage generation and the power consumption. If the voltage generation is optimized, then lower capacitors will be used, therefore the area is also optimized. Figure 58 shows the simulation of BBG with EGNCAP without FBB feedback with different clocks, where the red line is the case of 500 kHz, in green is the 1 MHz and in blue is the 2 MHz.

Another factor to notice about the simulations, is that if FBB feedback is used in the capacitors, the voltage generated is worse, then it is not a good strategy. In all cases, the setting time is worse than ideal case.

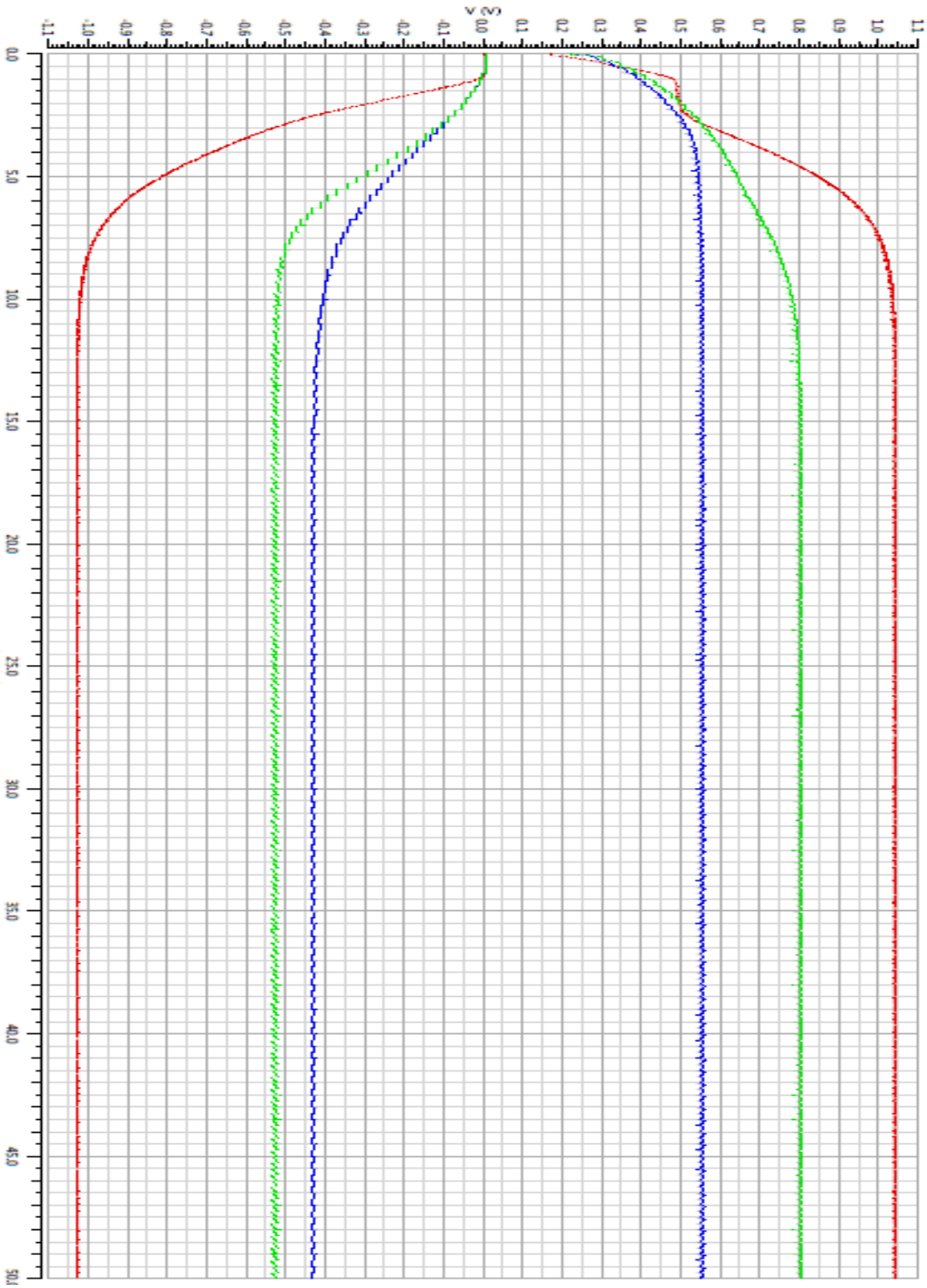

Figure 57. Simulation of the BBG with ideal capacitors (14.5 MHz) and real capacitors with and without FBB (2 MHz). Red line represents the BBG with ideal capacitor, the green line BBG with EGNCAP without FBB feedback and blue line BBG with EGNCAP with FBB feedback

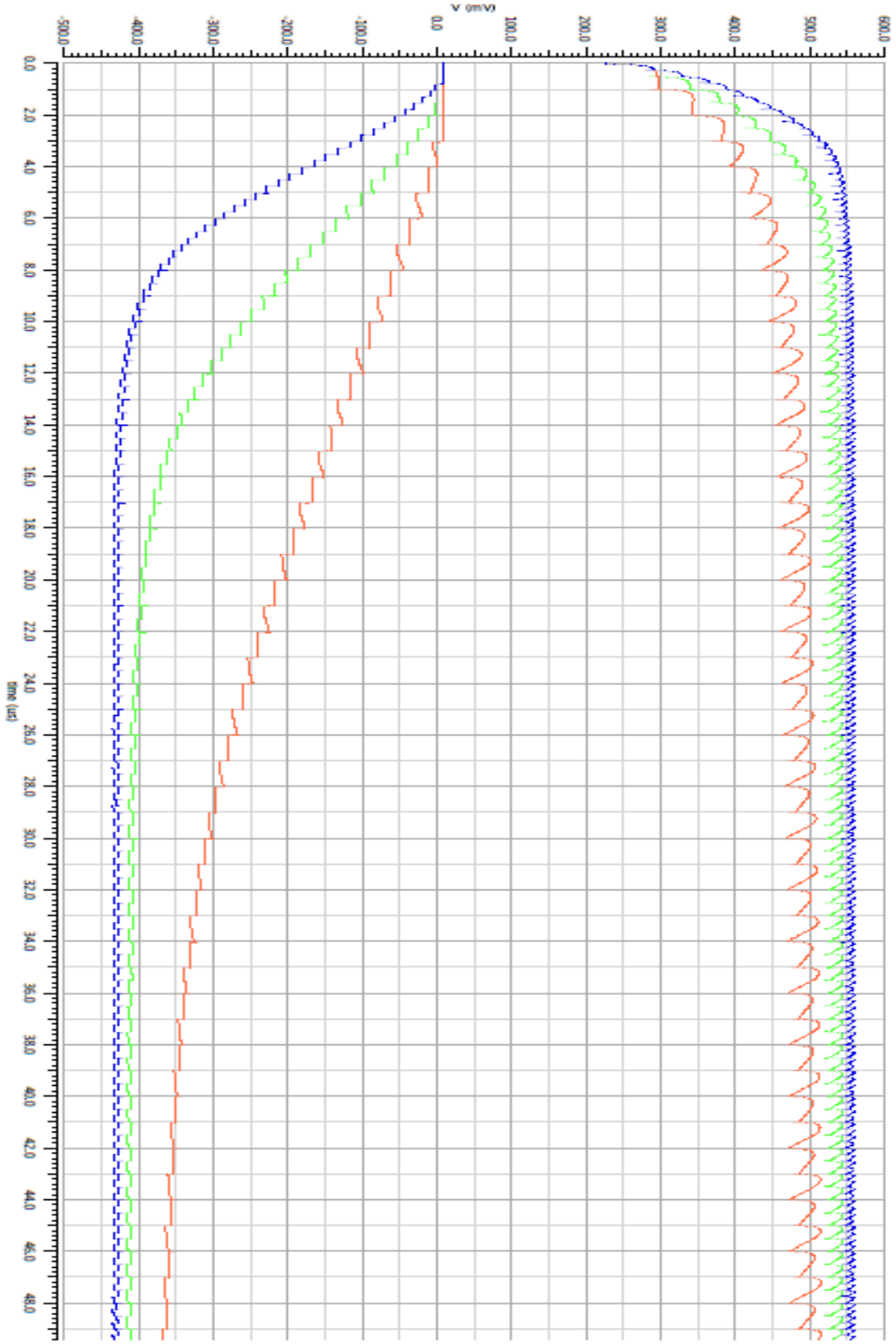

Figure 58. Simulation of BBG with real capacitor without FBB feedback for different frequency clocks. Red line represents the 500 kHz of clock's frequency, green line is for 1MHz and blue line for 2 MHz

9

COSTS: A FINANCIAL STUDY OF THESIS

9.1. Introduction

In this Chapter, a financial study about the development of the project. It is important study to do before a project starts, to forecast the costs of cost and the viability of a project.

It is important to differentiate the resources used for the development of the project. The first category of resources are the material resources, which includes from software until the office. The second category is the personal resources, which refers to the people who works in the project. For this project, all the cost are estimated for the duration of the thesis, 8 months from July 2017 until February 2018, because the material resources are provided by the university and the personal resources are the author of this thesis and the advisor.

9.2. Cost of Material Resources

In the case of the material resources, Table XI explain an estimation of cost. For the office, a desktop on a coworking office is selected, because all the basic services, as internet and electricity, are included. To design the model are needed a computer and the software license of Cadence. In this case the license of Cadence is based in the academic price of the Universitat Politècnica de Catalunya. If the license is required by an enterprise, the cost is higher. The total costs estimated for the material resources is 3071 €.

Table XI. Costs of material resources

Material Resources	Cost	Quantity	Total
Office [25]	272,25 €	8	2.178,00 €
Computer+ monitor [26]	700,00 €	1	700,00 €
Software License: Cadence (1 year)	193,00 €	1	193,00 €

9.3. Cost of Personal Resources

Table XII resume the personal cost of the project. In this case, the resource is only one engineer junior and the gross monthly salary is estimated based on the data obtained in [27]. In the cost of the salary, it is also important to include the cost of tax of the Social Security, which is paid by the enterprise. The tax is usually between 31% and 35%, using in this case the intermediate value of 33% [28]. In the personal resources, the advisor could be added, but the estimation of costs in this cases in very difficult.

Table XII. Cost of personal resources.

Personal Resource	Gross monthly salary	Social Security (33%)	Months	Total
Engineer Junior	1.984,00 €	654,72 €	8	21.109,76 €

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CONCLUSION

In this thesis proposal, an electrical model of Body Bias Generator, BBG, and its Control Circuit based in 28nm UTBB FDSOI is presented. Forward Body Bias allows to improve the performance of ultra-low power design, 300 mV of voltage supply, enabling more complex design with drastically reduction of power consumption. This proposal exploits the advantage of charge pumps to implement the voltage generator on the same Integrated Circuit as the application device. It also exploit the excellent body bias range of 28 UTBB FDSOI to take advantage of the different range of voltage generated. The following can be concluded from the thesis proposal:

- The design use Charge Pump circuits for body bias generation of ±1 V from a voltage supply 300 mV.
- The body bias generated can be applied to application designs to improve the performance of the circuits, allowing to work a higher frequencies, few hundred of MHz.
- It is demonstrated the dramatically improving of the performance of BBG when the body bias is feedback into its circuitry, providing best results of voltage generation with low power consumption and small capacities.
- It is important to design the BBG with the smaller capacitors, because it is the main factor of the size of the circuit. The optimization of area is important to the integration of the circuit inside the IC where forward body bias is required.
- The power consumption of the optimized design is lower than 1 μW, coming down to 351 nW in the simulated circuit. It makes the design suitable for portable devices or to use self-power sources of energy, as harvesting generation.
- The replacement of the ideal capacitors by real capacitors, in this case by EGNCAP, is not easy to implement. All the circuit has to be optimized for the new behavior of the capacitors, to achieve the body bias generation with low power consumption and the smaller area required.
- The circuit is controlled digitally, managing several voltages from the BBG. The structure of the Control Circuit eases the scalability to provide a great number of intermediate voltages. The digital control eases the control of voltage generation by the application circuits.
- Manage the voltage generated is important to improve the power consumption. With the control, the maximum voltage provided by the BBG could be avoided, greatly reducing the power consumption of the last steps of the body bias generation.

As future work, the ideal capacitors has to be replaced by real models. It could be important characterize the different capacitors provided by the 28 nm UTBB FDSOI technology to find the best option to obtain the required body bias, ±1 V, occupying the smaller area possible.

After select and design the best model of capacitor for the BBG, the next step is to design the layout with the specified dimensions. In layout process, more parasitic effects are extracted in simulations, providing better information about the real model of capacitors. If the simulations of layout are correct, the body bias circuit could be fabricated and tested.

Another future task are the improvement of the Control Circuit, reducing the power consumption and the area required. Also an analog circuit of control should be a good option, enabling fine tuning of the body bias.

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